

Rev: 1.0

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Elitegroup Computer Systems
Cover Sheet

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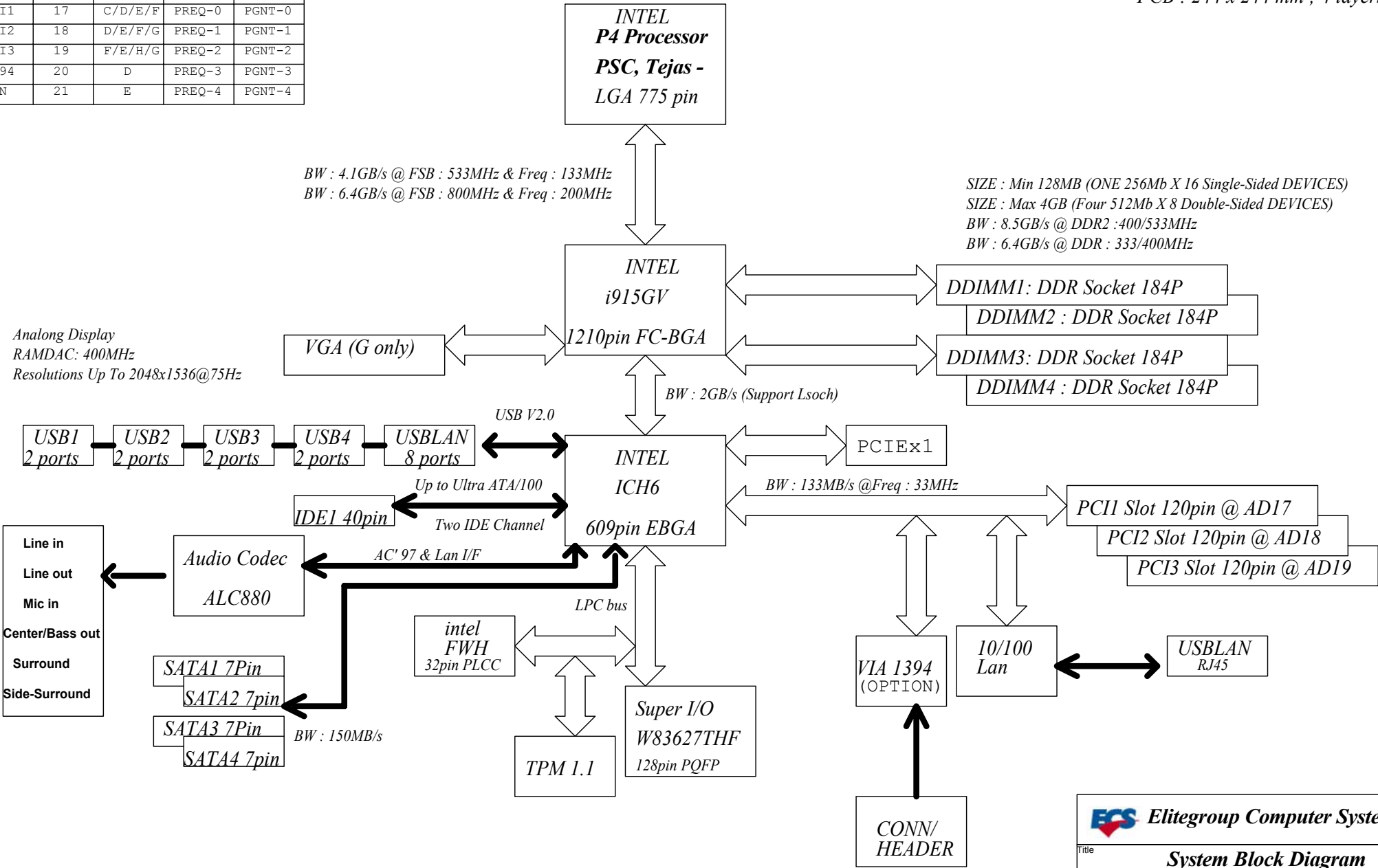
DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
PCI3	19	F/E/H/G	PREQ-2	PGNT-2
1394	20	D	PREQ-3	PGNT-3
LAN	21	E	PREQ-4	PGNT-4

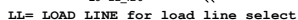
PCB : 244 x 244 mm ; 4 layers

BW : 4.1GB/s @ FSB : 533MHz & Freq : 133MHz
BW : 6.4GB/s @ FSB : 800MHz & Freq : 200MHz

SIZE : Min 128MB (ONE 256Mb X 16 Single-Sided DEVICES)
SIZE : Max 4GB (Four 512Mb X 8 Double-Sided DEVICES)
BW : 8.5GB/s @ DDR2 : 400/533MHz
BW : 6.4GB/s @ DDR : 333/400MHz

Analog Display
RAMDAC: 400MHz
Resolutions Up To 2048x1536@75Hz





COMP2 ER85 100-1

COMP3 ER101 100-1

VTT OUT L

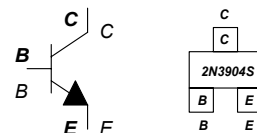
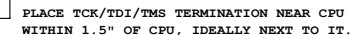
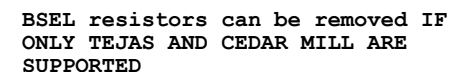
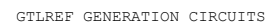
OVTT_OUT_L

BC145

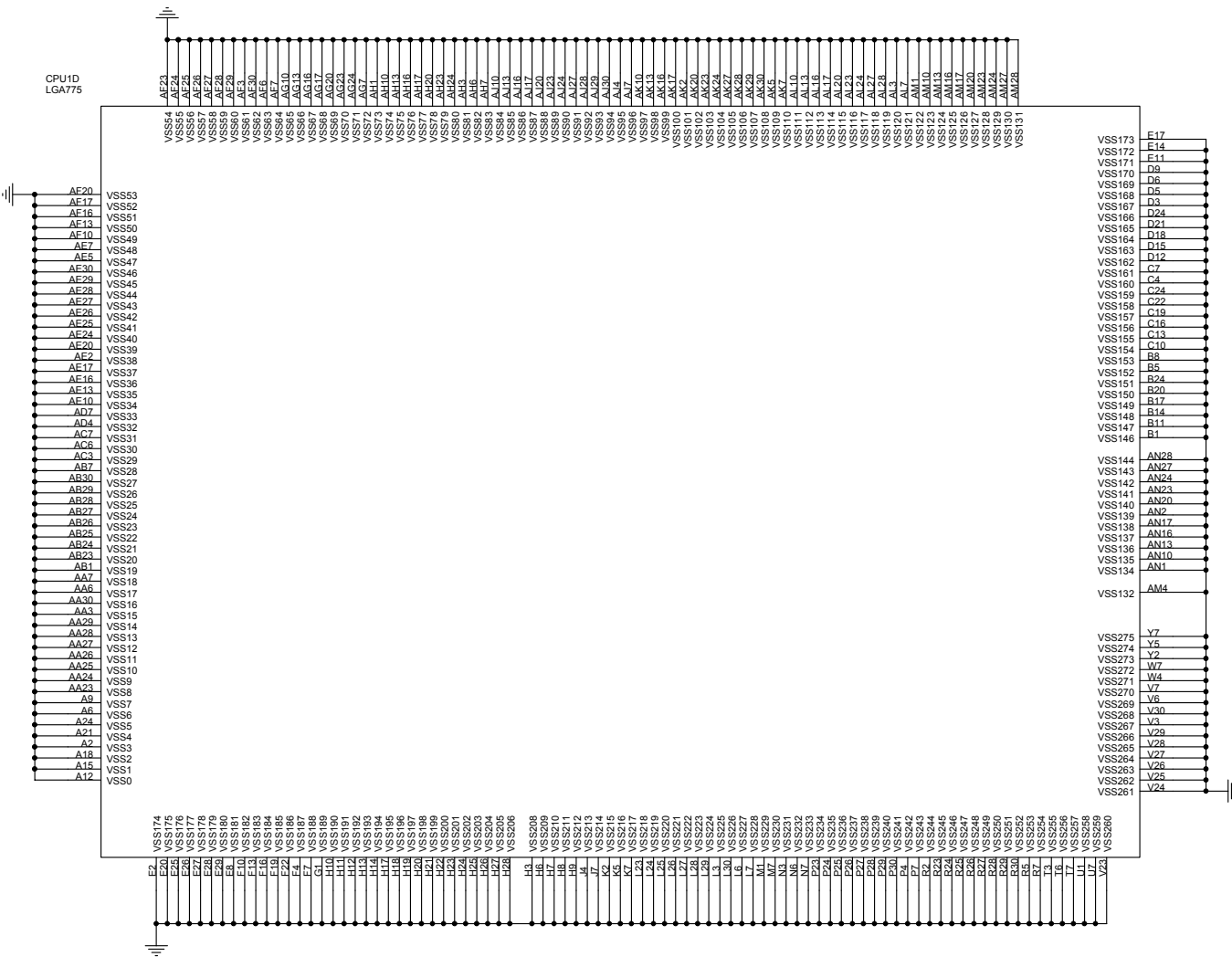
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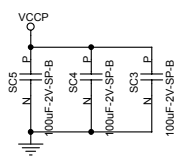
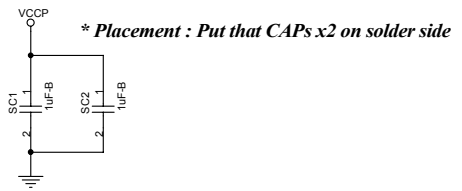
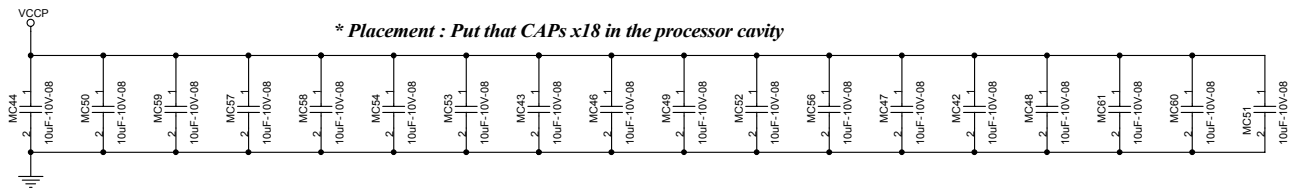
Layout need closed CPU

The diagram shows two horizontal lines representing the output bus. The top line is labeled 'COMP0' and the bottom line is labeled 'COMP1'. Each line has a resistor symbol (a zigzag line) connected to it, with 'ER60' and 'ER100' written above the resistors. To the right of each resistor is the value '60.4-1'. The lines continue to the right, where they meet a common vertical line representing the output bus. A ground symbol is connected to this common line.

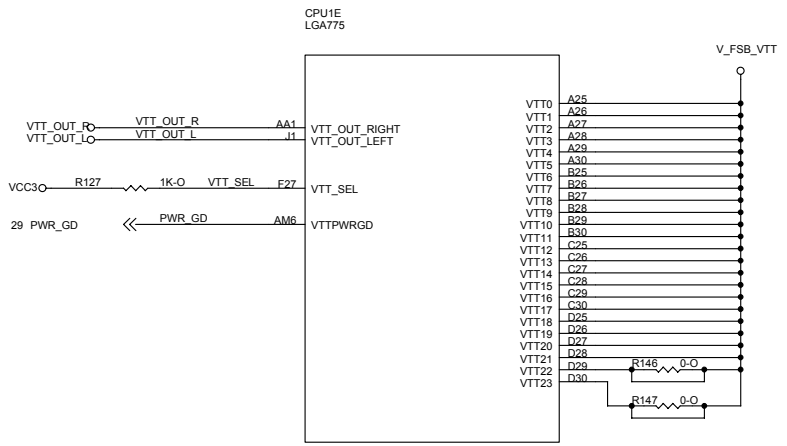


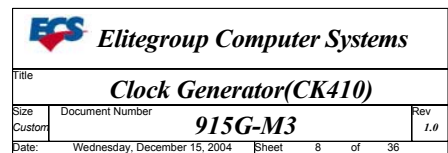
CPU1C
LGA775





VTT_SEL=0 for the Tejas processor





3 H_D0	H_D0	J33	H_D0#
3 H_D1	H_D1	J34	H_D1#
3 H_D2	H_D2	J35	H_D2#
3 H_D3	H_D3	J36	H_D3#
3 H_D4	H_D4	J37	H_D4#
3 H_D5	H_D5	J38	H_D5#
3 H_D6	H_D6	J39	H_D6#
3 H_D7	H_D7	J40	H_D7#
3 H_D8	H_D8	J41	H_D8#
3 H_D9	H_D9	J42	H_D9#
3 H_D10	H_D10	J43	H_D10#
3 H_D11	H_D11	J44	H_D11#
3 H_D12	H_D12	J45	H_D12#
3 H_D13	H_D13	J46	H_D13#
3 H_D14	H_D14	J47	H_D14#
3 H_D15	H_D15	J48	H_D15#
3 H_D16	H_D16	J49	H_D16#
3 H_D17	H_D17	J50	H_D17#
3 H_D18	H_D18	J51	H_D18#
3 H_D19	H_D19	J52	H_D19#
3 H_D20	H_D20	J53	H_D20#
3 H_D21	H_D21	J54	H_D21#
3 H_D22	H_D22	J55	H_D22#
3 H_D23	H_D23	J56	H_D23#
3 H_D24	H_D24	J57	H_D24#
3 H_D25	H_D25	J58	H_D25#
3 H_D26	H_D26	J59	H_D26#
3 H_D27	H_D27	J60	H_D27#
3 H_D28	H_D28	J61	H_D28#
3 H_D29	H_D29	J62	H_D29#
3 H_D30	H_D30	J63	H_D30#
3 H_D31	H_D31	J64	H_D31#
3 H_D32	H_D32	J65	H_D32#
3 H_D33	H_D33	J66	H_D33#
3 H_D34	H_D34	J67	H_D34#
3 H_D35	H_D35	J68	H_D35#
3 H_D36	H_D36	J69	H_D36#
3 H_D37	H_D37	J70	H_D37#
3 H_D38	H_D38	J71	H_D38#
3 H_D39	H_D39	J72	H_D39#
3 H_D40	H_D40	J73	H_D40#
3 H_D41	H_D41	J74	H_D41#
3 H_D42	H_D42	J75	H_D42#
3 H_D43	H_D43	J76	H_D43#
3 H_D44	H_D44	J77	H_D44#
3 H_D45	H_D45	J78	H_D45#
3 H_D46	H_D46	J79	H_D46#
3 H_D47	H_D47	J80	H_D47#
3 H_D48	H_D48	J81	H_D48#
3 H_D49	H_D49	J82	H_D49#
3 H_D50	H_D50	J83	H_D50#
3 H_D51	H_D51	J84	H_D51#
3 H_D52	H_D52	J85	H_D52#
3 H_D53	H_D53	J86	H_D53#
3 H_D54	H_D54	J87	H_D54#
3 H_D55	H_D55	J88	H_D55#
3 H_D56	H_D56	J89	H_D56#
3 H_D57	H_D57	J90	H_D57#
3 H_D58	H_D58	J91	H_D58#
3 H_D59	H_D59	J92	H_D59#
3 H_D60	H_D60	J93	H_D60#
3 H_D61	H_D61	J94	H_D61#
3 H_D62	H_D62	J95	H_D62#
3 H_D63	H_D63	J96	H_D63#

HA3#	H29	HA3	H_A3
HA4#	H30	HA4	H_A4
HA5#	H31	HA5	H_A5
HA6#	H32	HA6	H_A6
HA7#	H33	HA7	H_A7
HA8#	H34	HA8	H_A8
HA9#	H35	HA9	H_A9
HA10#	H36	HA10	H_A10
HA11#	H37	HA11	H_A11
HA12#	H38	HA12	H_A12
HA13#	H39	HA13	H_A13
HA14#	H40	HA14	H_A14
HA15#	H41	HA15	H_A15
HA16#	H42	HA16	H_A16
HA17#	H43	HA17	H_A17
HA18#	H44	HA18	H_A18
HA19#	H45	HA19	H_A19
HA20#	H46	HA20	H_A20
HA21#	H47	HA21	H_A21
HA22#	H48	HA22	H_A22
HA23#	H49	HA23	H_A23
HA24#	H50	HA24	H_A24
HA25#	H51	HA25	H_A25
HA26#	H52	HA26	H_A26
HA27#	H53	HA27	H_A27
HA28#	H54	HA28	H_A28
HA29#	H55	HA29	H_A29
HA30#	H56	HA30	H_A30
HA31#	H57	HA31	H_A31

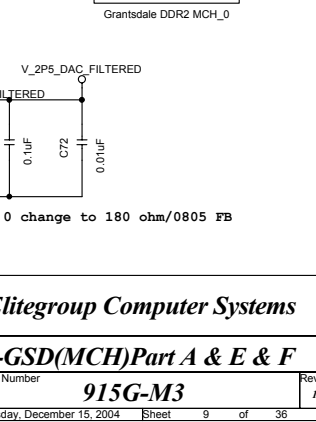
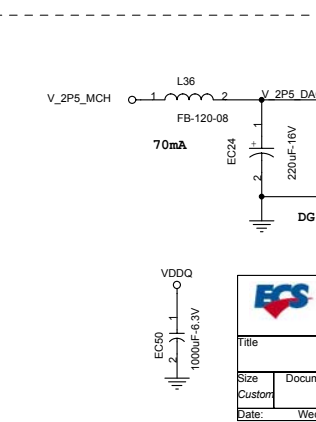
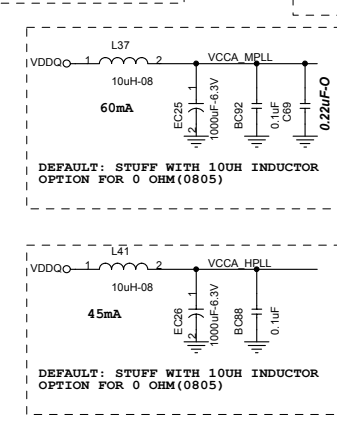
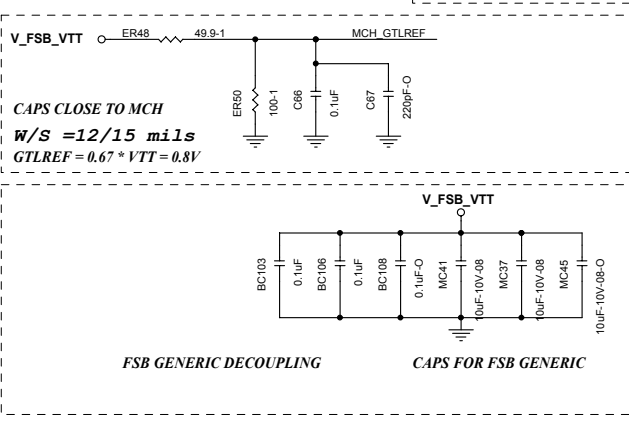
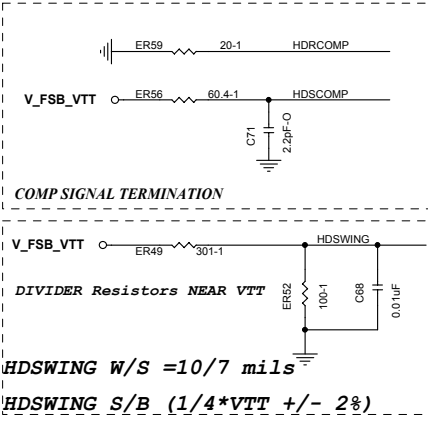
HREO0#	H REO0	H_REO0	3
HREO1#	H REO1	H_REO1	3
HREO2#	H REO2	H_REO2	3
HREO3#	H REO3	H_REO3	3
HREO4#	H REO4	H_REO4	3
HREO5#	H REO5	H_REO5	3
HREO6#	H REO6	H_REO6	3
HREO7#	H REO7	H_REO7	3
HREO8#	H REO8	H_REO8	3
HREO9#	H REO9	H_REO9	3
HREO10#	H REO10	H_REO10	3
HREO11#	H REO11	H_REO11	3
HREO12#	H REO12	H_REO12	3
HREO13#	H REO13	H_REO13	3
HREO14#	H REO14	H_REO14	3
HREO15#	H REO15	H_REO15	3
HREO16#	H REO16	H_REO16	3
HREO17#	H REO17	H_REO17	3
HREO18#	H REO18	H_REO18	3
HREO19#	H REO19	H_REO19	3
HREO20#	H REO20	H_REO20	3
HREO21#	H REO21	H_REO21	3
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HREO29#	H REO29	H_REO29	3
HREO30#	H REO30	H_REO30	3
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HREO35#	H REO35	H_REO35	3
HREO36#	H REO36	H_REO36	3
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HREO46#	H REO46	H_REO46	3
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HREO57#	H REO57	H_REO57	3
HREO58#	H REO58	H_REO58	3
HREO59#	H REO59	H_REO59	3
HREO60#	H REO60	H_REO60	3
HREO61#	H REO61	H_REO61	3
HREO62#	H REO62	H_REO62	3
HREO63#	H REO63	H_REO63	3

V_FSB_VTT	H22	VTT	3
V_FSB_VTT	H23	VTT	3
V_FSB_VTT	H24	VTT	3
V_FSB_VTT	H25	VTT	3
V_FSB_VTT	H26	VTT	3
V_FSB_VTT	H27	VTT	3
V_FSB_VTT	H28	VTT	3
V_FSB_VTT	H29	VTT	3
V_FSB_VTT	H30	VTT	3
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V_FSB_VTT	H63	VTT	3

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V_FSB_VTT	H37	VTT	3
V_FSB_VTT	H38	VTT	3
V_FSB_VTT	H39	VTT	3
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V_FSB_VTT	H41	VTT	3
V_FSB_VTT	H42	VTT	3
V_FSB_VTT	H43	VTT	3
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V_FSB_VTT	H45	VTT	3
V_FSB_VTT	H46	VTT	3
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V_FSB_VTT	H51	VTT	3
V_FSB_VTT	H52	VTT	3
V_FSB_VTT	H53	VTT	3
V_FSB_VTT	H54	VTT	3
V_FSB_VTT	H55	VTT	3
V_FSB_VTT	H56	VTT	3
V_FSB_VTT	H57	VTT	3
V_FSB_VTT	H58	VTT	3
V_FSB_VTT	H59	VTT	3
V_FSB_VTT	H60	VTT	3
V_FSB_VTT	H61	VTT	3
V_FSB_VTT	H62	VTT	3
V_FSB_VTT	H63	VTT	3

BSEL TABLE	
2 1 0	FSB FREQUENCY
0 0 1	133 MHz (533)
0 1 0	200 MHz (800)



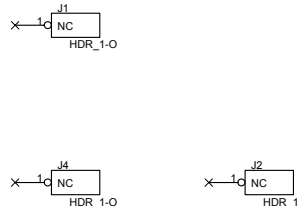
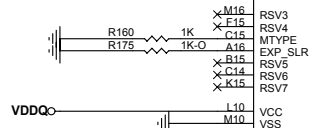
Elitegroup Computer Systems

Title			Rev 1.0
I-GSD(MCH)Part A & E & F			
Size	Document Number	915G-M3	
Customer	Date: Wednesday, December 15, 2004		Sheet 9 of 36

16 EXP_A_RXP_0 < EXP_A_RXP_0 F11
 16 EXP_A_RXN_0 < EXP_A_RXN_0 F11
 16 EXP_A_RXP_1 < EXP_A_RXP_1 H11
 16 EXP_A_RXN_1 < EXP_A_RXN_1 F9
 16 EXP_A_RXP_2 < EXP_A_RXP_2 F9
 16 EXP_A_RXN_2 < EXP_A_RXN_2 F9
 16 EXP_A_RXP_3 < EXP_A_RXP_3 F7
 16 EXP_A_RXN_3 < EXP_A_RXN_3 F7
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 16 EXP_A_RXN_5 < EXP_A_RXN_5 D5
 16 EXP_A_RXP_6 < EXP_A_RXP_6 G6
 16 EXP_A_RXN_6 < EXP_A_RXN_6 G6
 16 EXP_A_RXP_7 < EXP_A_RXP_7 H8
 16 EXP_A_RXN_7 < EXP_A_RXN_7 H8
 16 EXP_A_RXP_8 < EXP_A_RXP_8 J6
 16 EXP_A_RXN_8 < EXP_A_RXN_8 J6
 16 EXP_A_RXP_9 < EXP_A_RXP_9 K8
 16 EXP_A_RXN_9 < EXP_A_RXN_9 K8
 16 EXP_A_RXP_10 < EXP_A_RXP_10 L6
 16 EXP_A_RXN_10 < EXP_A_RXN_10 L6
 16 EXP_A_RXP_11 < EXP_A_RXP_11 P10
 16 EXP_A_RXN_11 < EXP_A_RXN_11 P10
 16 EXP_A_RXP_12 < EXP_A_RXP_12 M6
 16 EXP_A_RXN_12 < EXP_A_RXN_12 M6
 16 EXP_A_RXP_13 < EXP_A_RXP_13 N6
 16 EXP_A_RXN_13 < EXP_A_RXN_13 N6
 16 EXP_A_RXP_14 < EXP_A_RXP_14 P8
 16 EXP_A_RXN_14 < EXP_A_RXN_14 P8
 16 EXP_A_RXP_15 < EXP_A_RXP_15 R6
 16 EXP_A_RXN_15 < EXP_A_RXN_15 R6

18 DMI_RXP0 < DMI_RXP0 U5
 18 DMI_RXN0 < DMI_RXN0 U6
 18 DMI_RXP1 < DMI_RXP1 T9
 18 DMI_RXN1 < DMI_RXN1 T9
 18 DMI_RXP2 < DMI_RXP2 V7
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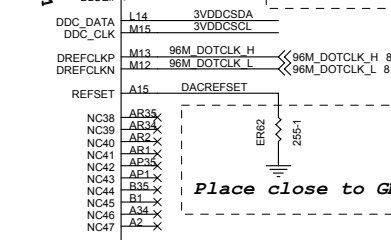
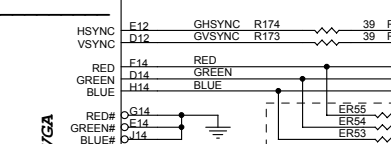
8 CK_PE_100M_MCH_H < CK_PE_100M_MCH_H A11
 8 CK_PE_100M_MCH_L < CK_PE_100M_MCH_L B11
 16 SDVO_CTRL_DATA < SDVO_CTRL_DATA K13
 16 SDVO_CTRL_CLK < SDVO_CTRL_CLK J13



EXP_TXP0 < EXP_A_TXP_0 C10
 EXP_TXN0 < EXP_A_TXN_0 C9
 EXP_TXP1 < EXP_A_TXP_1 A8
 EXP_TXN1 < EXP_A_TXN_1 A8
 EXP_TXP2 < EXP_A_TXP_2 C8
 EXP_TXN2 < EXP_A_TXN_2 C7
 EXP_TXP3 < EXP_A_TXP_3 A6
 EXP_TXN3 < EXP_A_TXN_3 A6
 EXP_TXP4 < EXP_A_TXP_4 C5
 EXP_TXN4 < EXP_A_TXN_4 C5
 EXP_TXP5 < EXP_A_TXP_5 D2
 EXP_TXN5 < EXP_A_TXN_5 D2
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 EXP_TXN6 < EXP_A_TXN_6 E3
 EXP_TXP7 < EXP_A_TXP_7 G1
 EXP_TXN7 < EXP_A_TXN_7 G1
 EXP_TXP8 < EXP_A_TXP_8 H3
 EXP_TXN8 < EXP_A_TXN_8 H3
 EXP_TXP9 < EXP_A_TXP_9 J1
 EXP_TXN9 < EXP_A_TXN_9 J1
 EXP_TXP10 < EXP_A_TXP_10 K3
 EXP_TXN10 < EXP_A_TXN_10 K3
 EXP_TXP11 < EXP_A_TXP_11 L1
 EXP_TXN11 < EXP_A_TXN_11 L1
 EXP_TXP12 < EXP_A_TXP_12 M3
 EXP_TXN12 < EXP_A_TXN_12 M3
 EXP_TXP13 < EXP_A_TXP_13 N1
 EXP_TXN13 < EXP_A_TXN_13 N1
 EXP_TXP14 < EXP_A_TXP_14 P3
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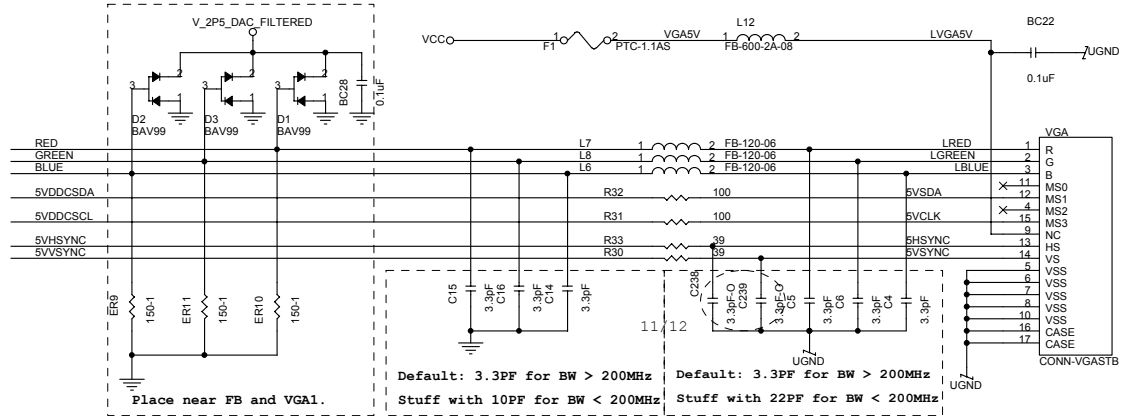
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 DMI_TXP2 < DMI_TXP2 U3
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 DMI_TXN3 < DMI_TXN3 W5

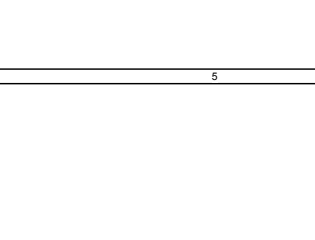
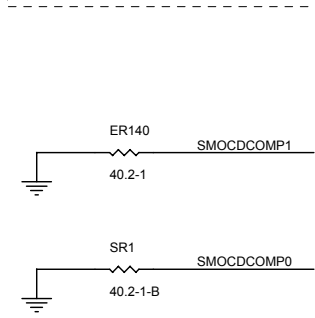
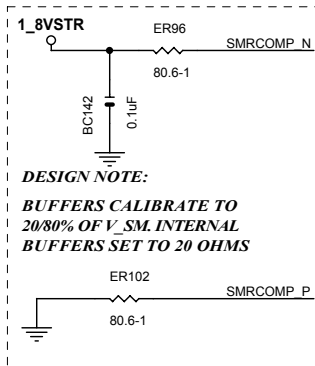
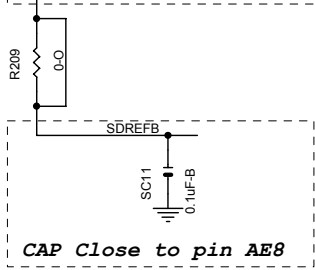
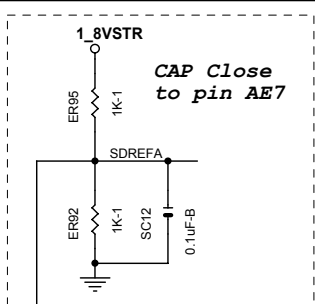
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 RSV9 < RSV9 G16
 RSV8 < RSV8 G16
 RSV8 < RSV8 G16
 RSTIN# < M14 PLTRST_L
 ICH_SYNC# < M14 ICH_SYNC_L

Grantsdale DDR2 MCH_0





MD A63	SDQ A63	T33
MD A62	SDQ A62	W33
MD A61	SDQ A61	W32
MD A60	SDQ A60	W31
MD A59	SDQ A59	W30
MD A58	SDQ A58	R38
MD A57	SDQ A57	V33
MD A56	SDQ A56	V32
MD A55	SDQ A55	V31
MD A54	SDQ A54	V30
MD A53	SDQ A53	V29
MD A52	SDQ A52	V28
MD A51	SDQ A51	V27
MD A50	SDQ A50	V26
MD A49	SDQ A49	V25
MD A48	SDQ A48	V24
MD A47	SDQ A47	V23
MD A46	SDQ A46	V22
MD A45	SDQ A45	V21
MD A44	SDQ A44	V20
MD A43	SDQ A43	V19
MD A42	SDQ A42	V18
MD A41	SDQ A41	V17
MD A40	SDQ A40	V16
MD A39	SDQ A39	V15
MD A38	SDQ A38	V14
MD A37	SDQ A37	V13
MD A36	SDQ A36	V12
MD A35	SDQ A35	V11
MD A34	SDQ A34	V10
MD A33	SDQ A33	V09
MD A32	SDQ A32	V08
MD A31	SDQ A31	V07
MD A30	SDQ A30	V06
MD A29	SDQ A29	V05
MD A28	SDQ A28	V04
MD A27	SDQ A27	V03
MD A26	SDQ A26	V02
MD A25	SDQ A25	V01
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MD A23	SDQ A23	V00
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MD A04	SDQ A04	V00
MD A03	SDQ A03	V00
MD A02	SDQ A02	V00
MD A01	SDQ A01	V00
MD A00	SDQ A00	V00


MD A63	SDQ A63	T33
MD A62	SDQ A62	W33
MD A61	SDQ A61	W32
MD A60	SDQ A60	W31
MD A59	SDQ A59	W30
MD A58	SDQ A58	R38
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MD A03	SDQ A03	V00
MD A02	SDQ A02	V00
MD A01	SDQ A01	V00
MD A00	SDQ A00	V00

MD A63	SDQ A63	T33
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MD A07	SDQ A07	V00
MD A06	SDQ A06	V00
MD A05	SDQ A05	V00
MD A04	SDQ A04	V00
MD A03	SDQ A03	V00
MD A02	SDQ A02	V00
MD A01	SDQ A01	V00
MD A00	SDQ A00	V00

MD A0[0..63]	MD A0[0..63]
DQS_L_A[0..7]	DQS_L_A[0..7]
DQS_H_A[0..7]	DQS_H_A[0..7]
MPD_A[0..7]	MPD_A[0..7]
MAAA[0..13]	MAAA[0..13]
CSA_L[0..3]	CSA_L[0..3]
CKEA[0..3]	CKEA[0..3]
DCLKA_L[0..5]	DCLKA_L[0..5]
DCLKA_H[0..5]	DCLKA_H[0..5]
ODTA[0..3]	ODTA[0..3]
SBSA[0..2]	SBSA[0..2]
SWE_L_A	SWE_L_A
SCAS_L_A	SCAS_L_A
SRAS_L_A	SRAS_L_A

MD B0[0..63]	MD B0[0..63]
DQS_L_B[0..7]	DQS_L_B[0..7]
DQS_H_B[0..7]	DQS_H_B[0..7]
MPD_B[0..7]	MPD_B[0..7]
MAAB[0..13]	MAAB[0..13]
CSB_L[0..3]	CSB_L[0..3]
CKEB[0..3]	CKEB[0..3]
DCLKB_L[0..5]	DCLKB_L[0..5]
DCLKB_H[0..5]	DCLKB_H[0..5]
ODTB[0..3]	ODTB[0..3]
SBSB[0..2]	SBSB[0..2]
SWE_L_B	SWE_L_B
SCAS_L_B	SCAS_L_B
SRAS_L_B	SRAS_L_B

MD B0[0..63]	MD B0[0..63]
DQS_L_B[0..7]	DQS_L_B[0..7]
DQS_H_B[0..7]	DQS_H_B[0..7]
MPD_B[0..7]	MPD_B[0..7]
MAAB[0..13]	MAAB[0..13]
CSB_L[0..3]	CSB_L[0..3]
CKEB[0..3]	CKEB[0..3]
DCLKB_L[0..5]	DCLKB_L[0..5]
DCLKB_H[0..5]	DCLKB_H[0..5]
ODTB[0..3]	ODTB[0..3]
SBSB[0..2]	SBSB[0..2]
SWE_L_B	SWE_L_B
SCAS_L_B	SCAS_L_B
SRAS_L_B	SRAS_L_B

**Elitegroup Computer Systems**

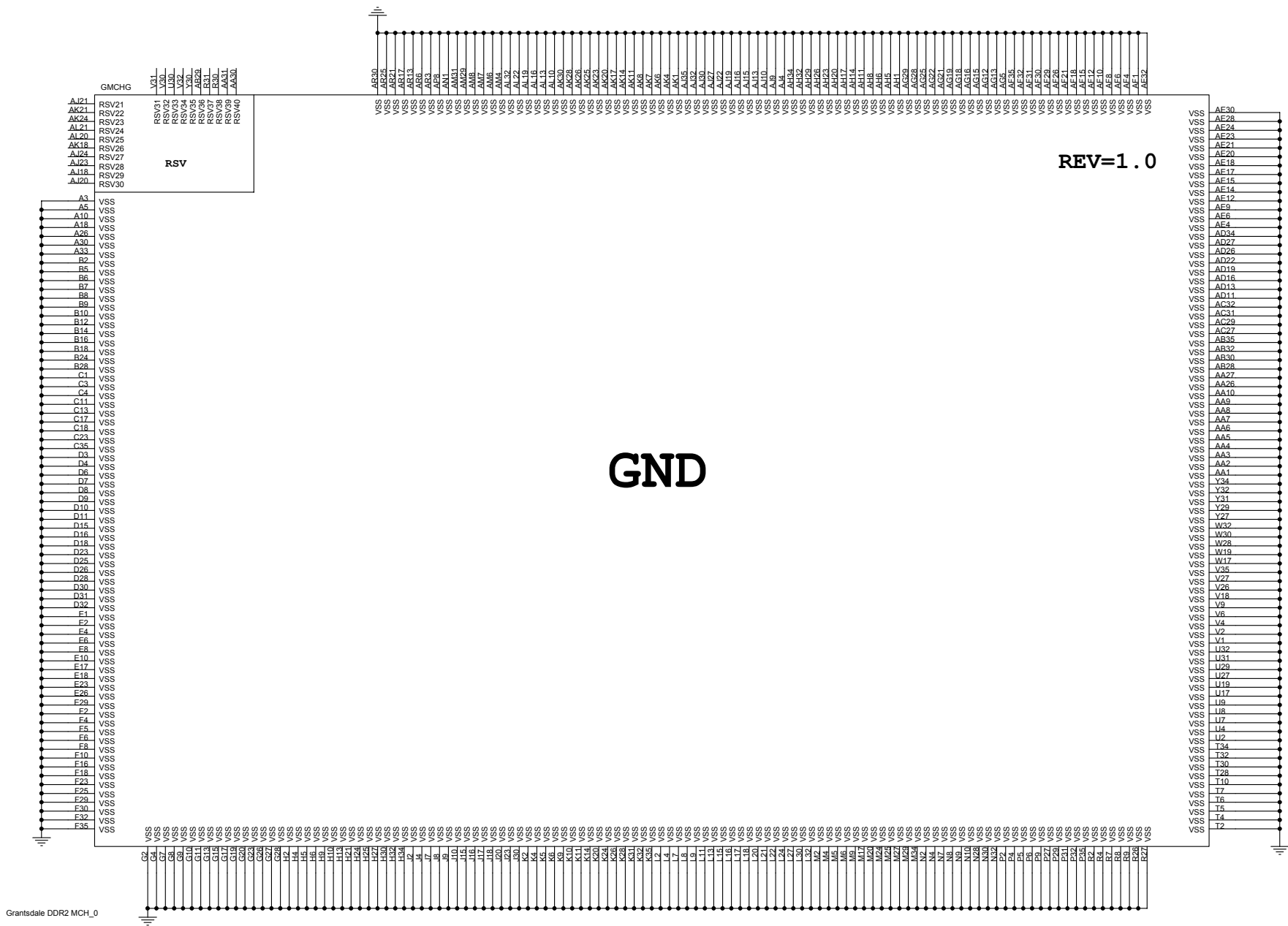
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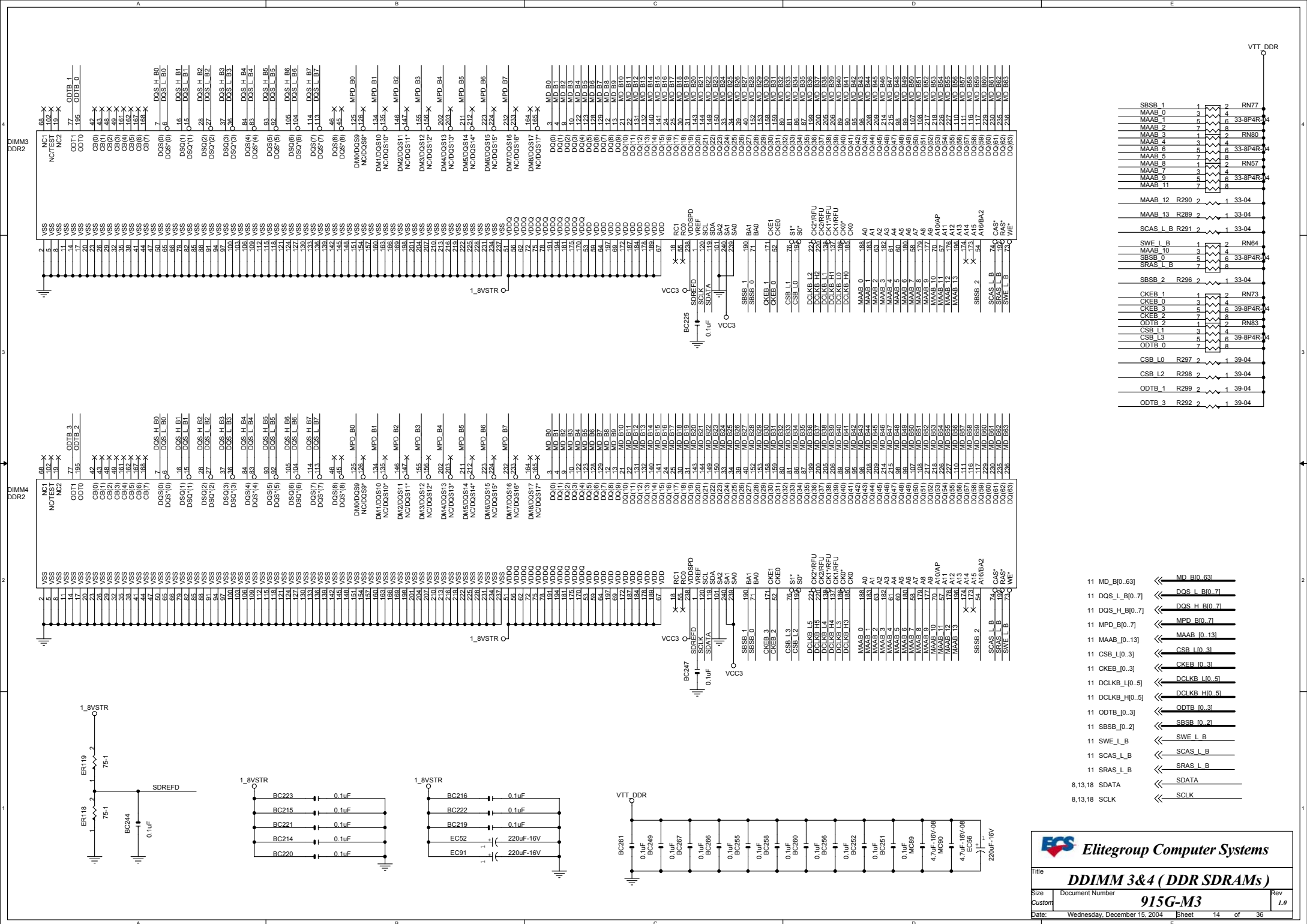
Rev 1.0

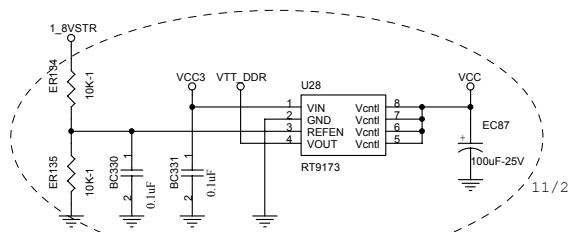
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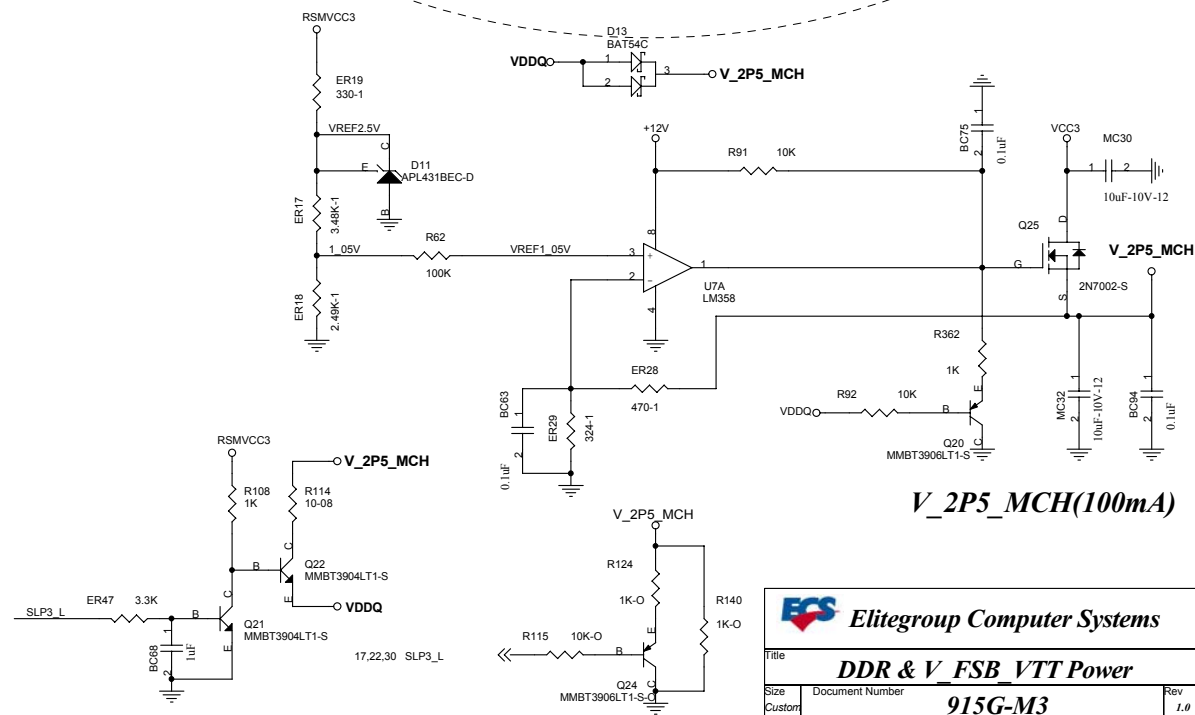
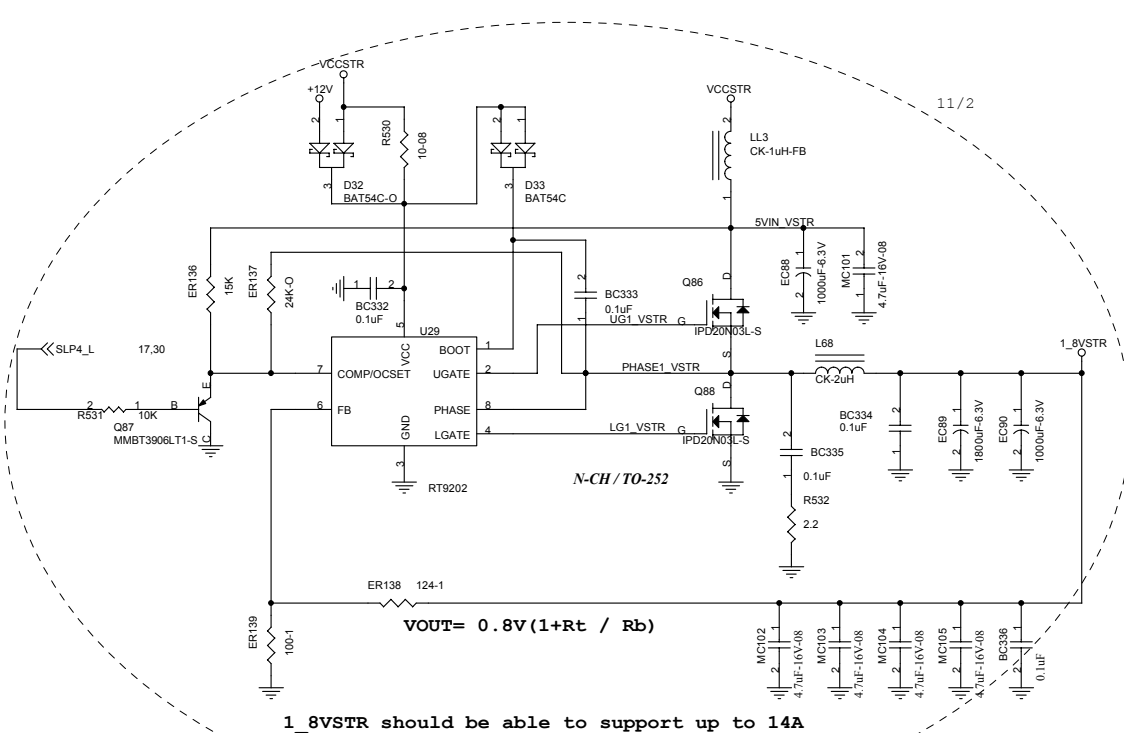
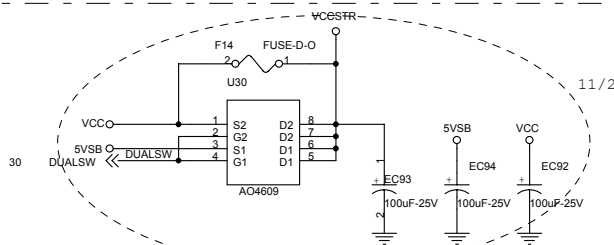
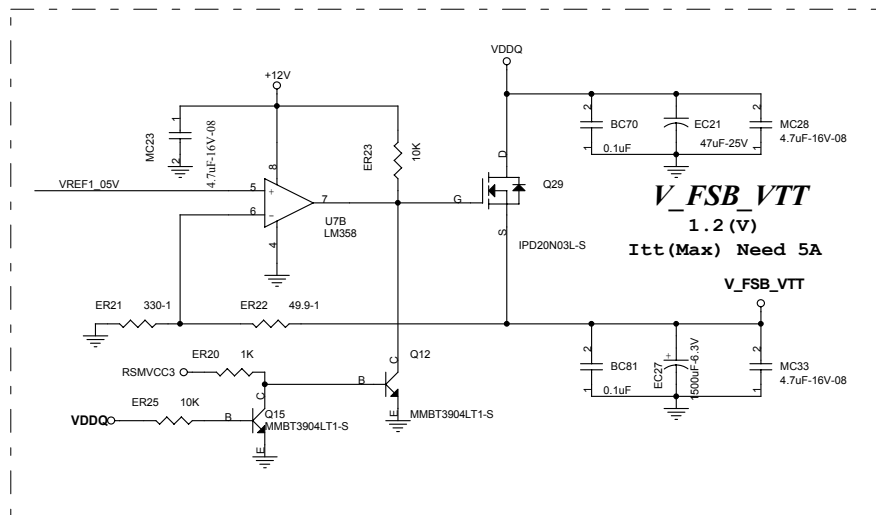
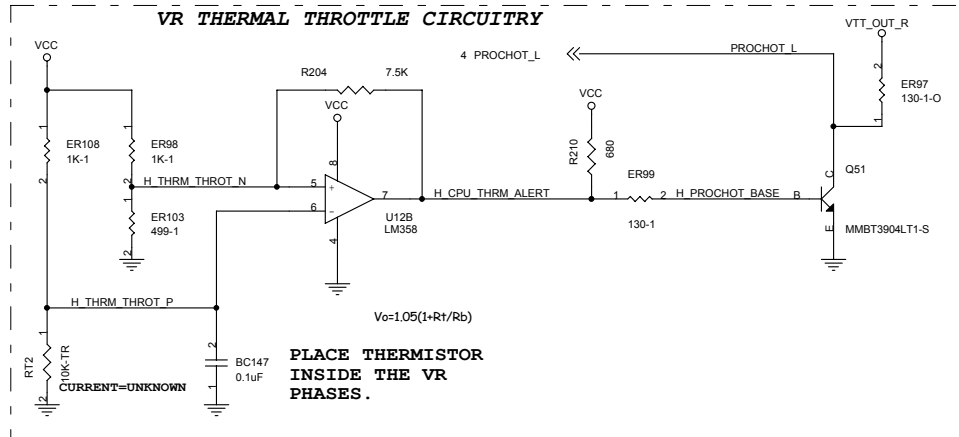
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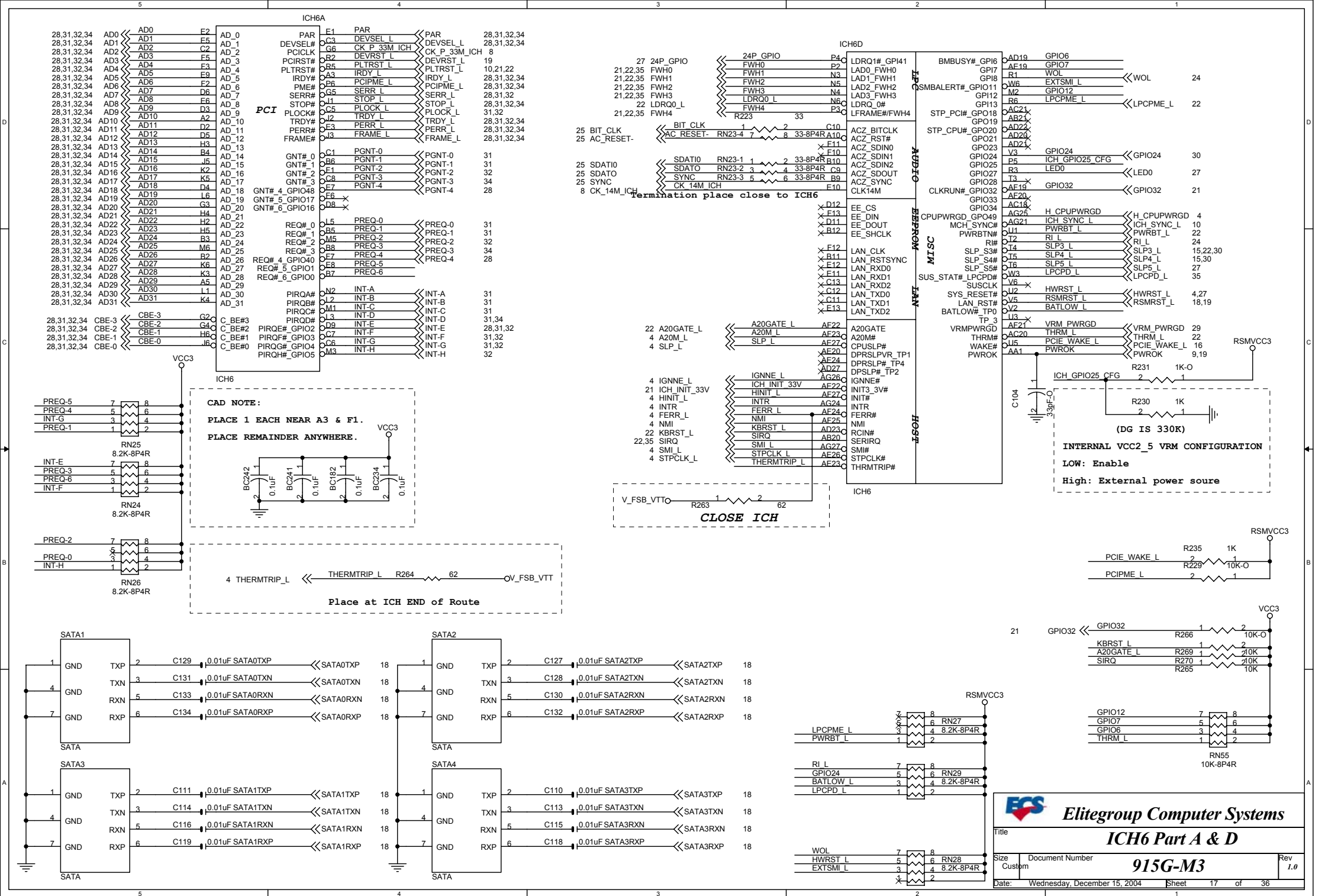


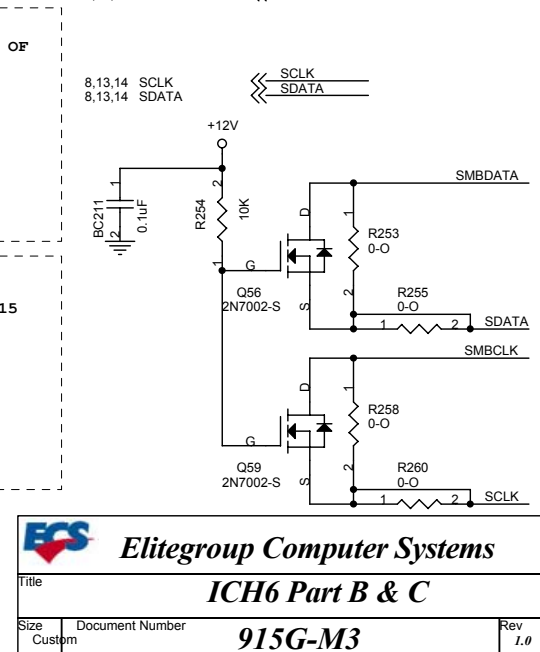
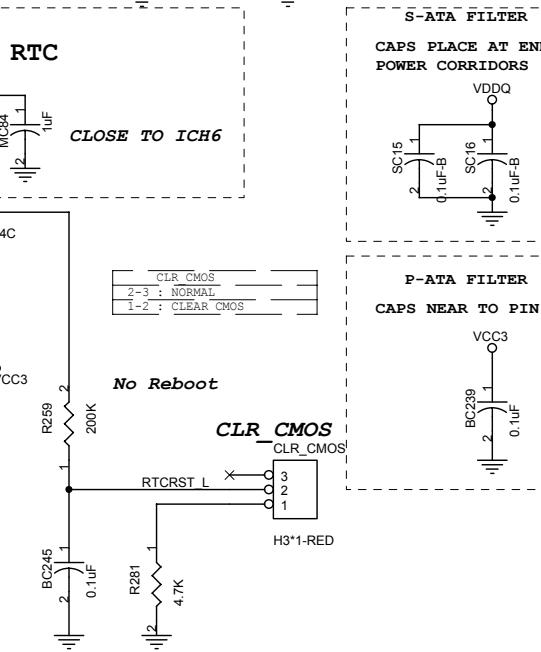
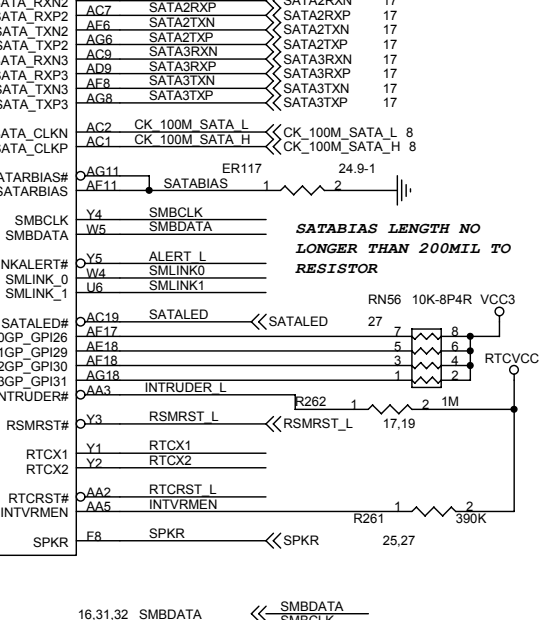
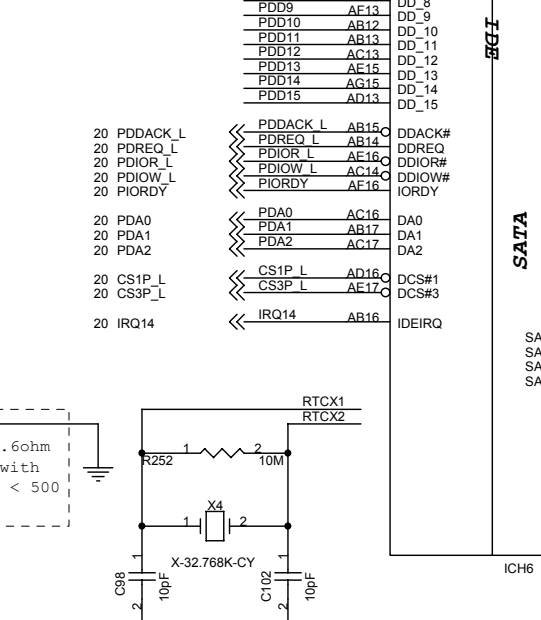
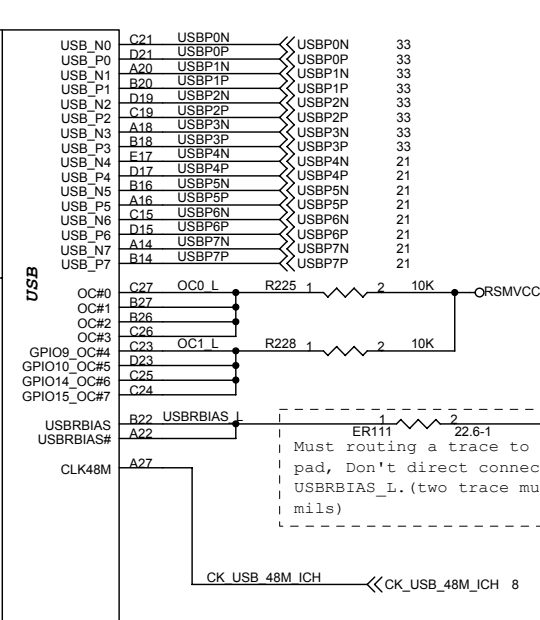
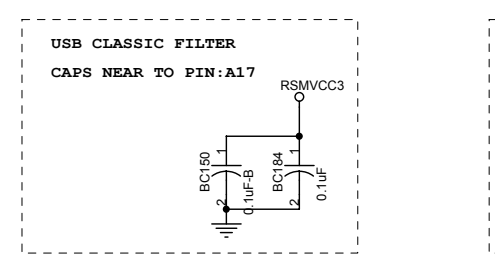
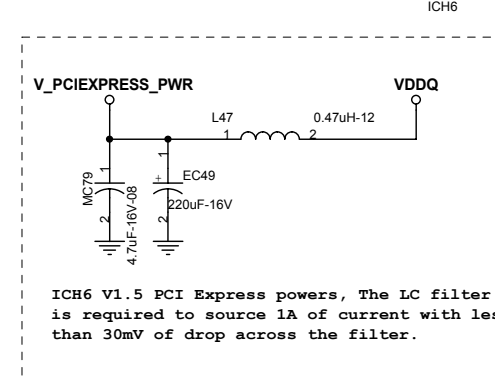
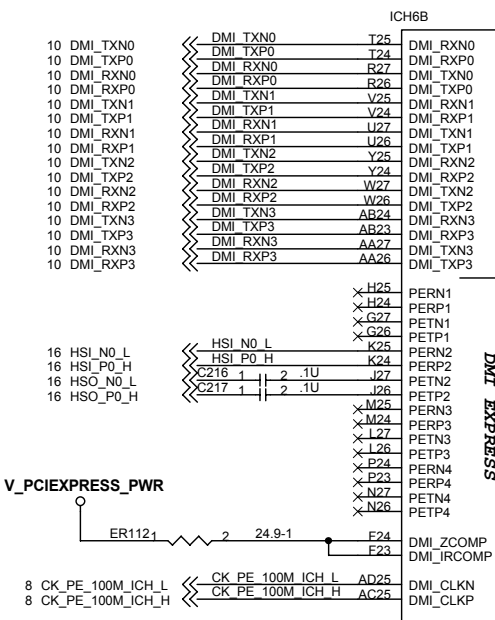


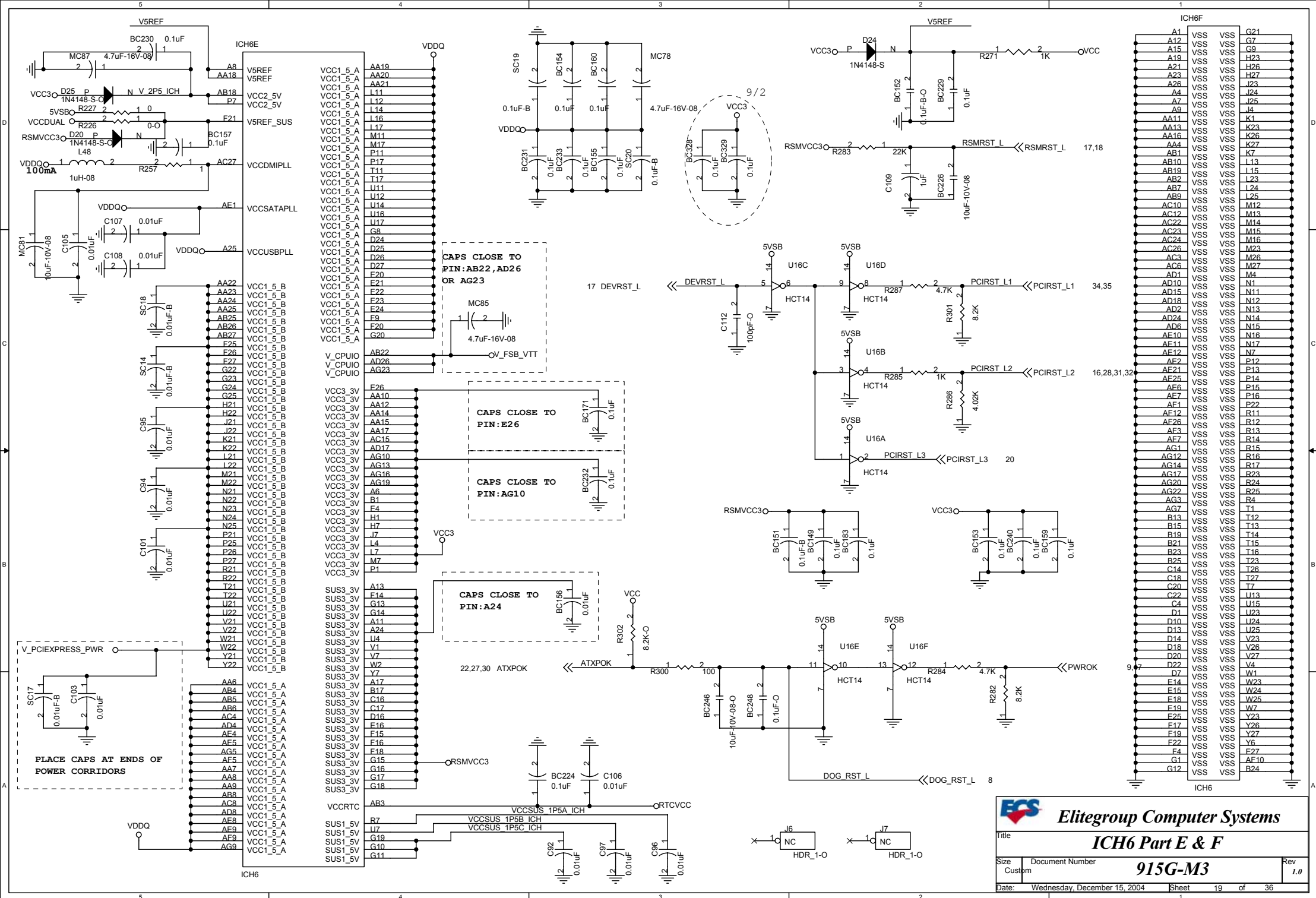


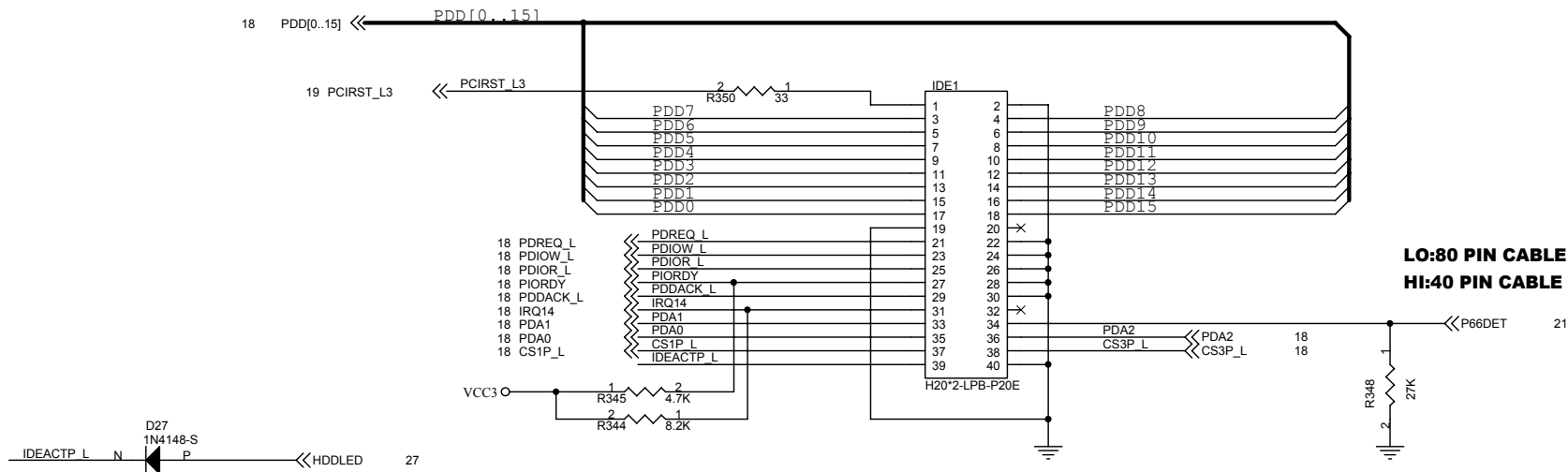
VR THERMAL THROTTLE CIRCUITRY










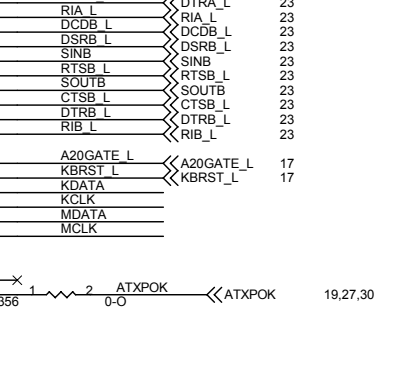
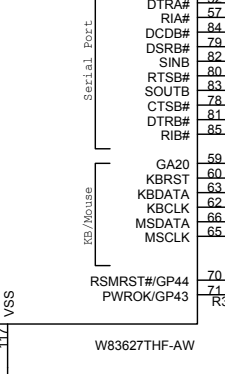
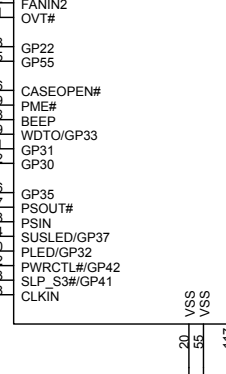
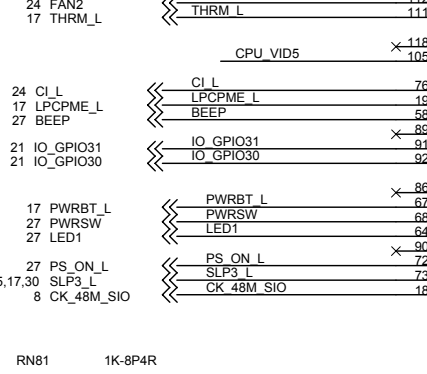
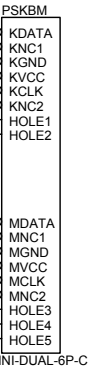
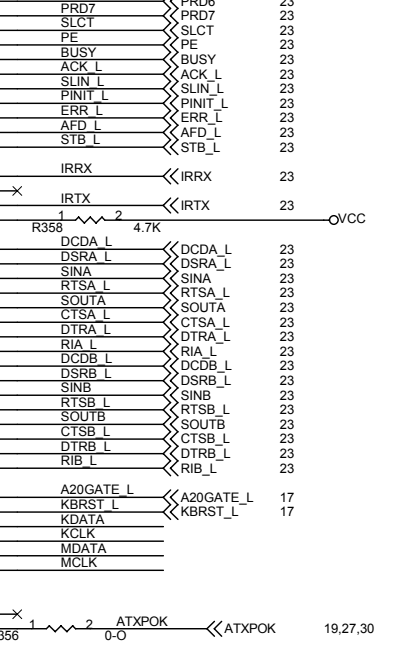
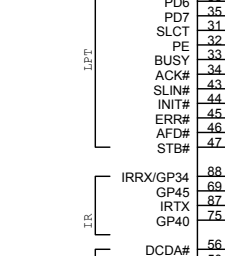
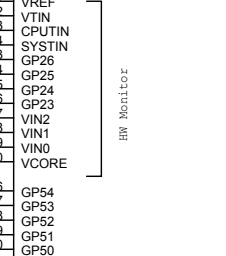
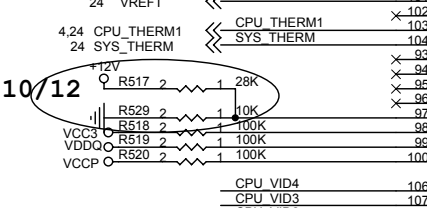
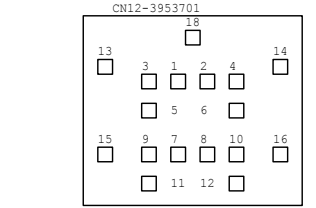
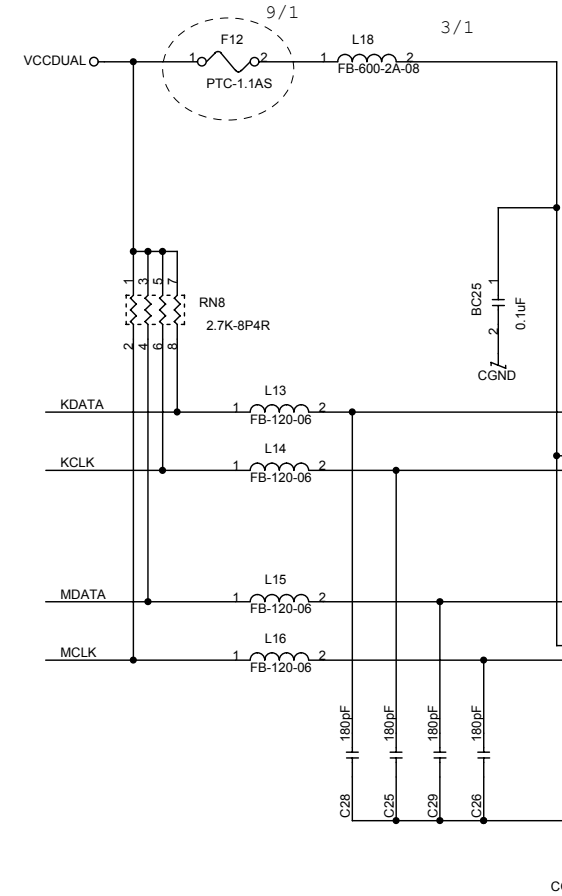
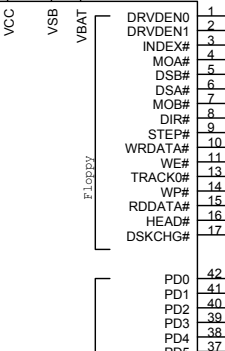
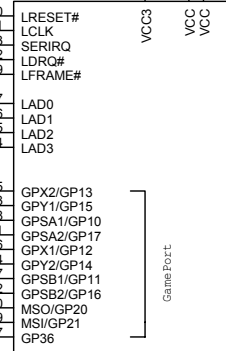
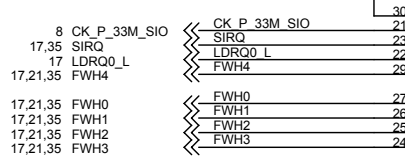
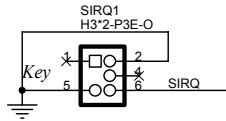
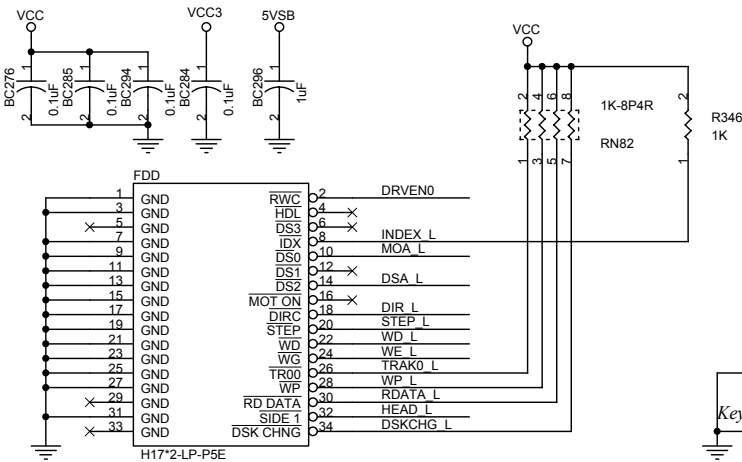


MAX TRACE LENGTH IS 8"

DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR_L , XIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.

[illegible]

 Elitegroup Computer Systems			
Title			
USB/FWH			
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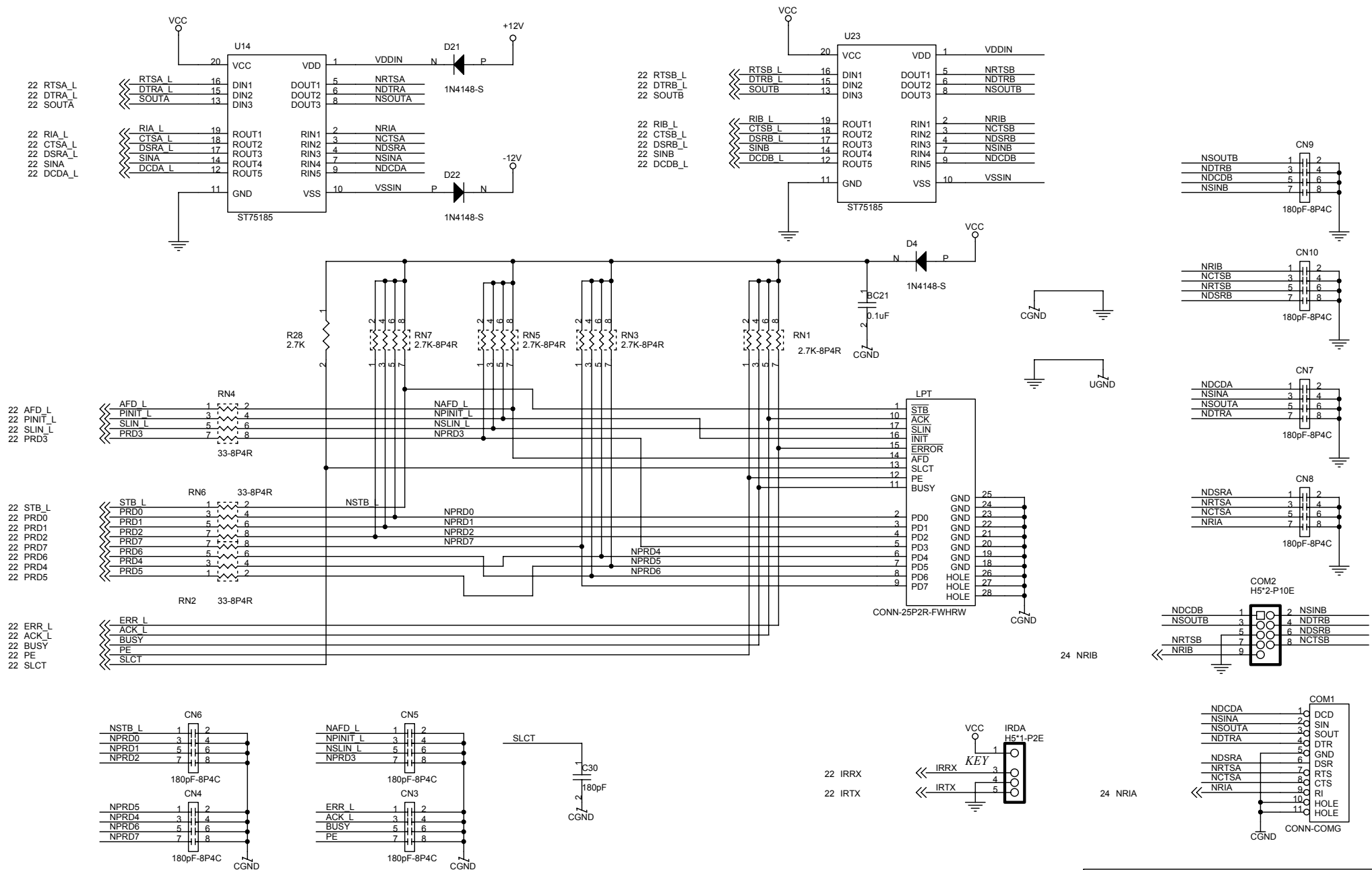


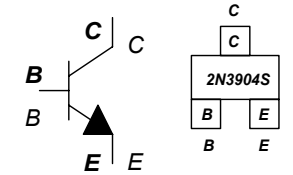
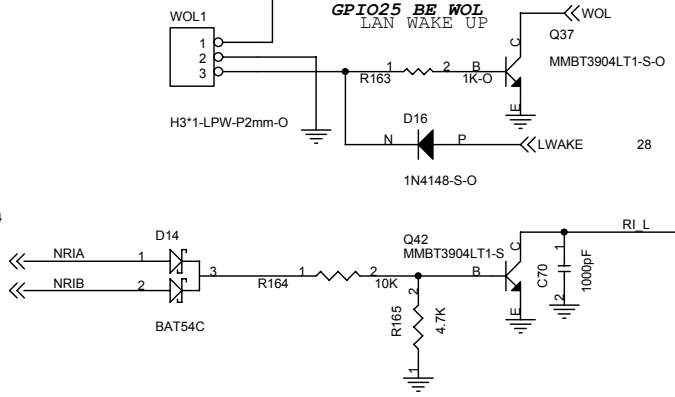
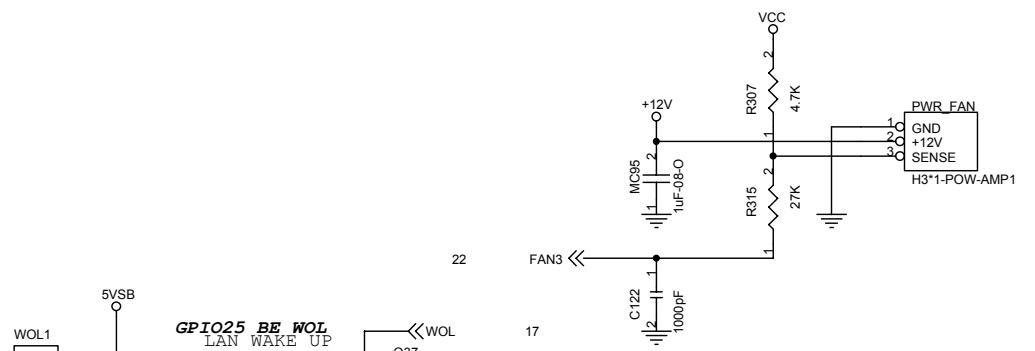
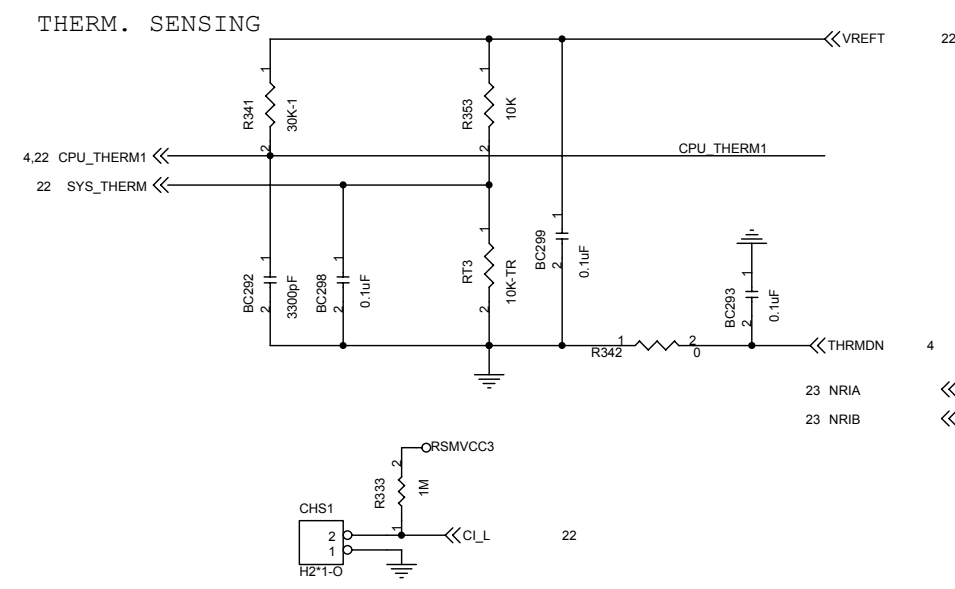
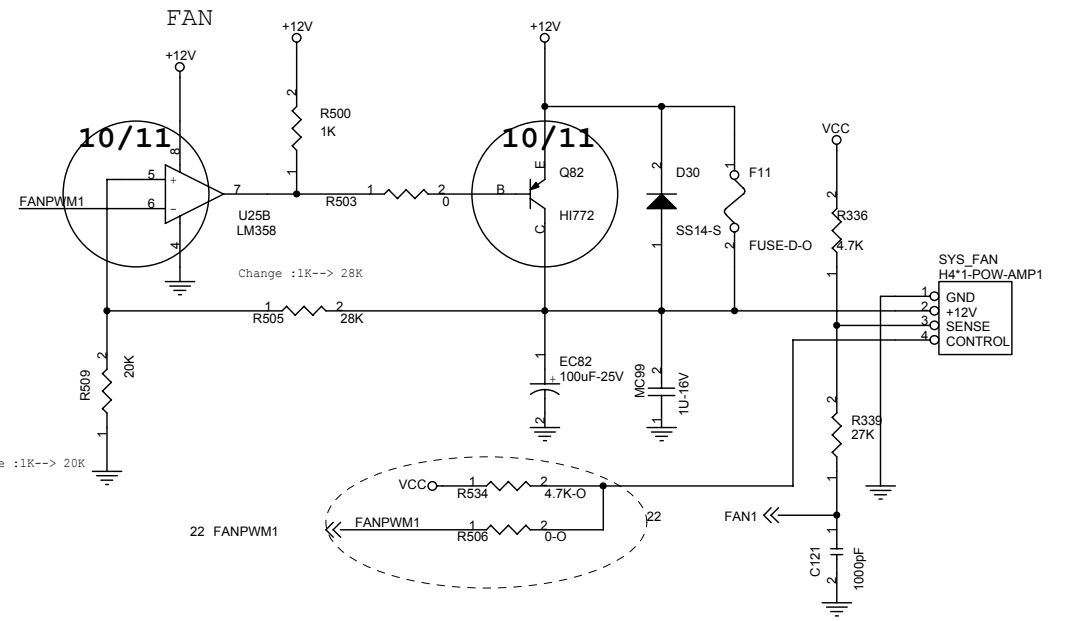
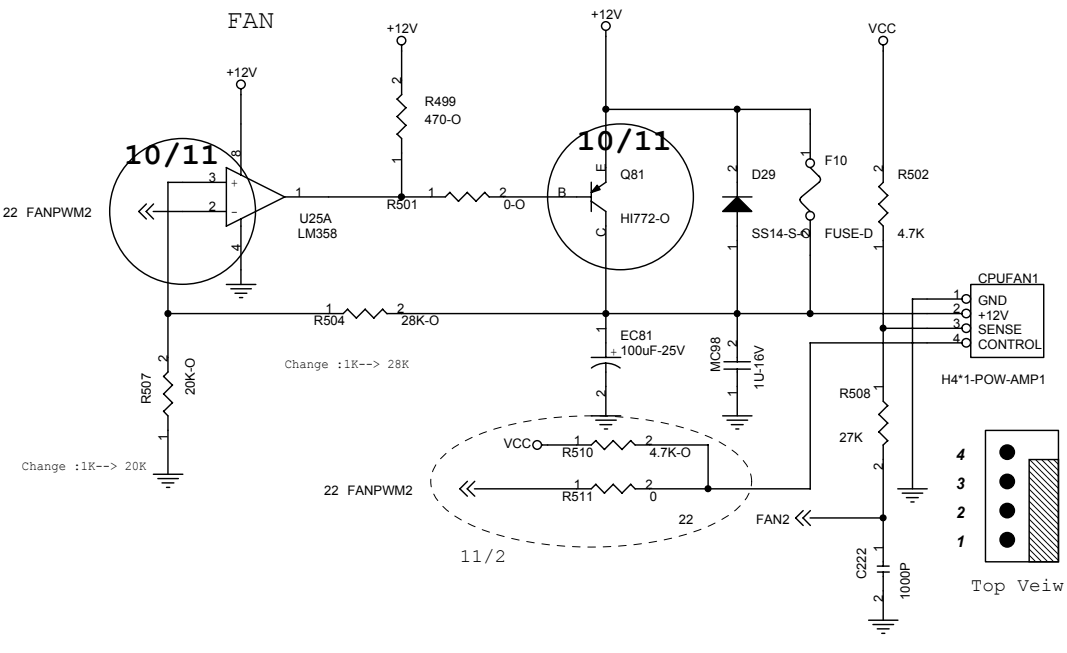
Elitegroup Computer Systems

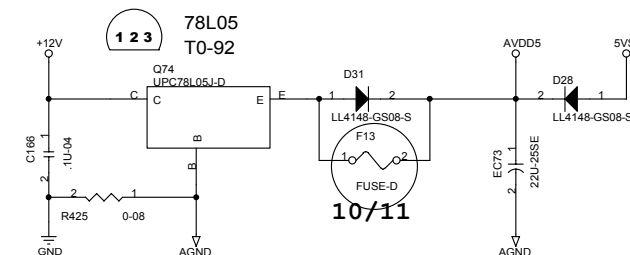
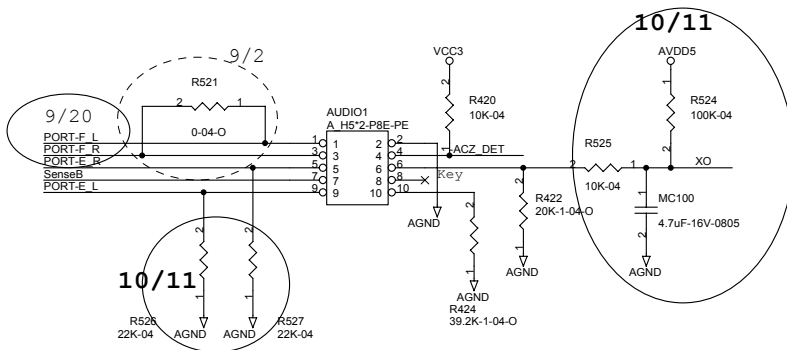
Title **LPC_FDD/KB/M**

Size Custom Document Number **915G-M3** Rev 1.0

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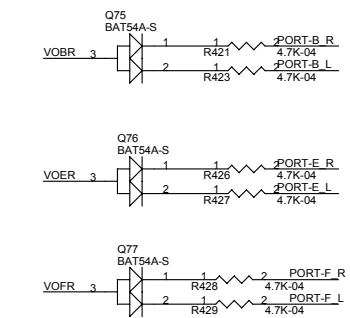




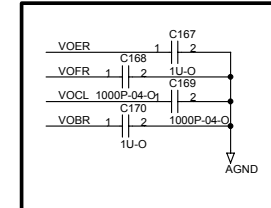


Verfout bias for stereo microphone.

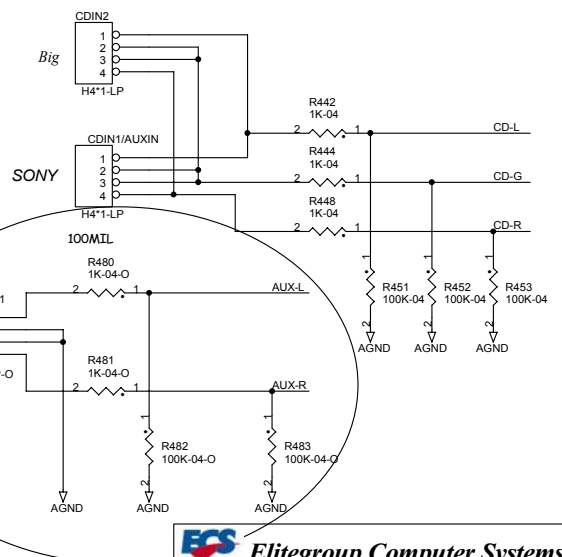
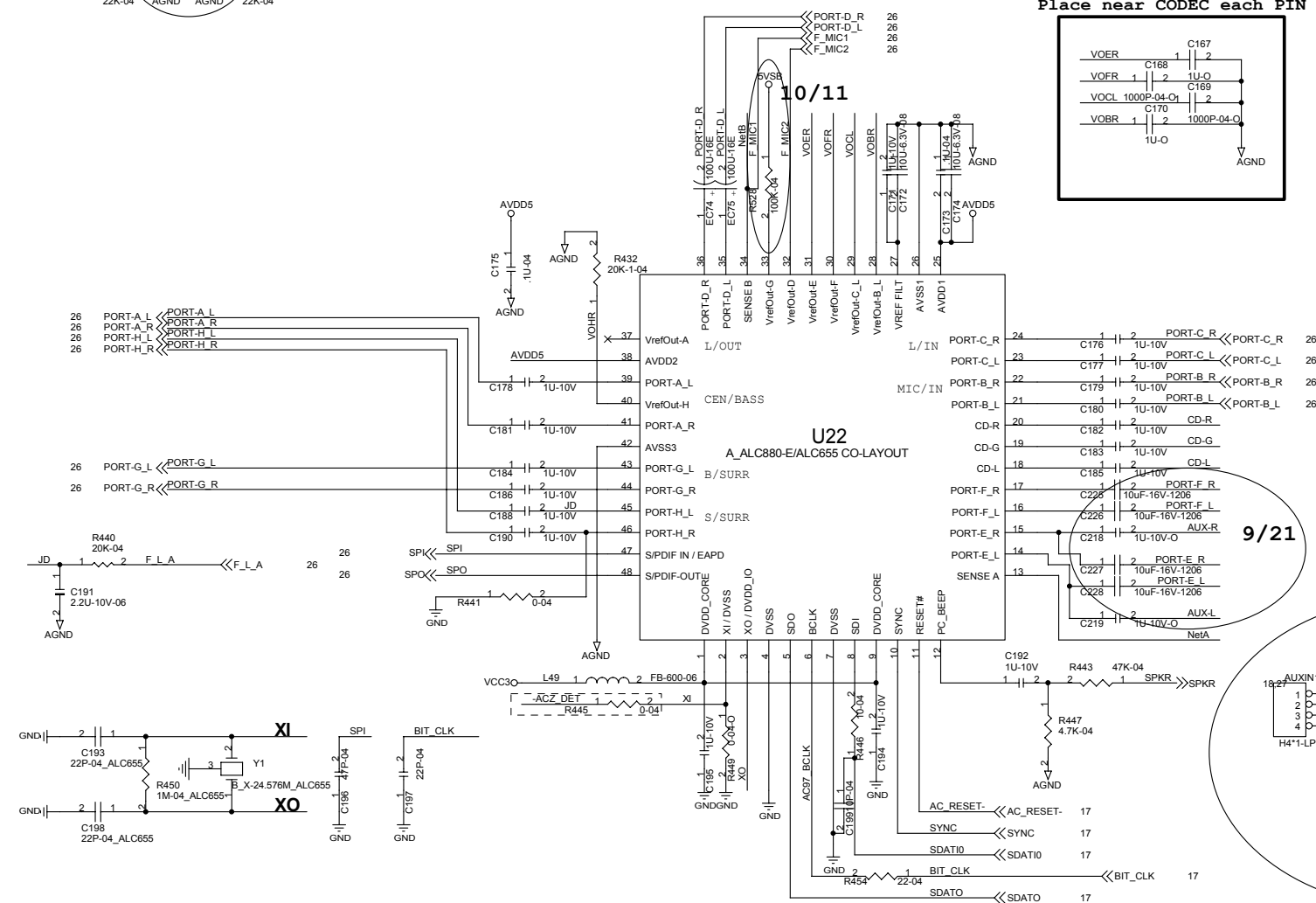
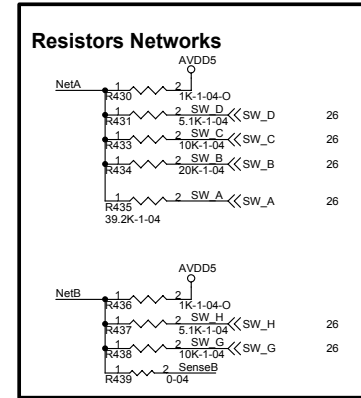
For CMI9880



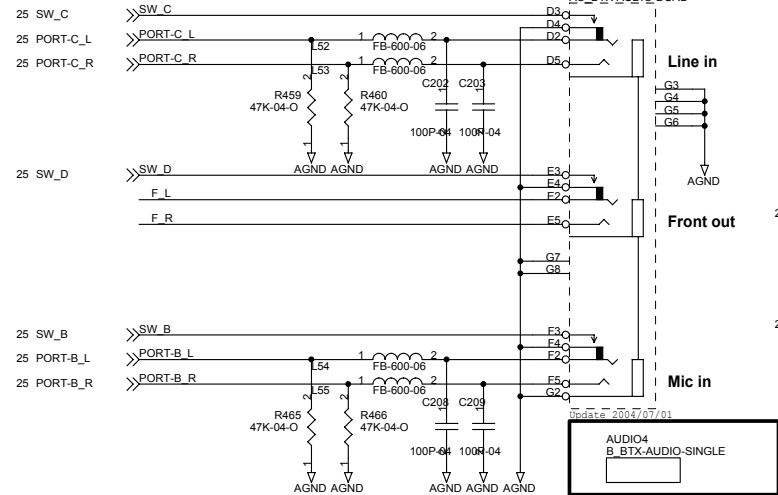
Place near CODEC each PIN



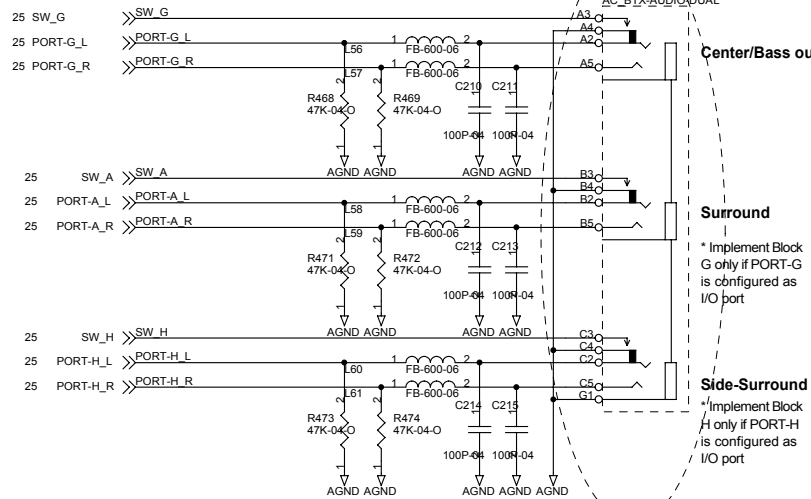
Place near Chip (U23)



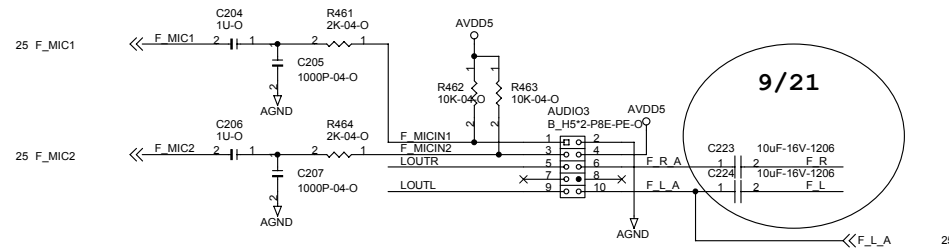
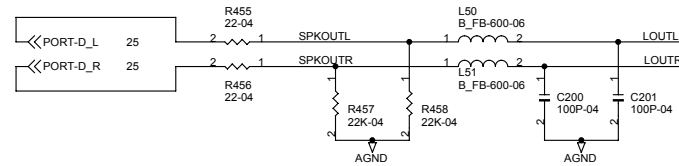
Rear Panel Onboard Analog I/O



Rear Panel (Optional Rear Audio Panel)

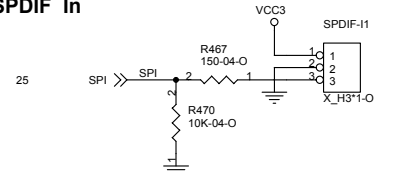


The schematic should consist with PINs define of I/O connector.

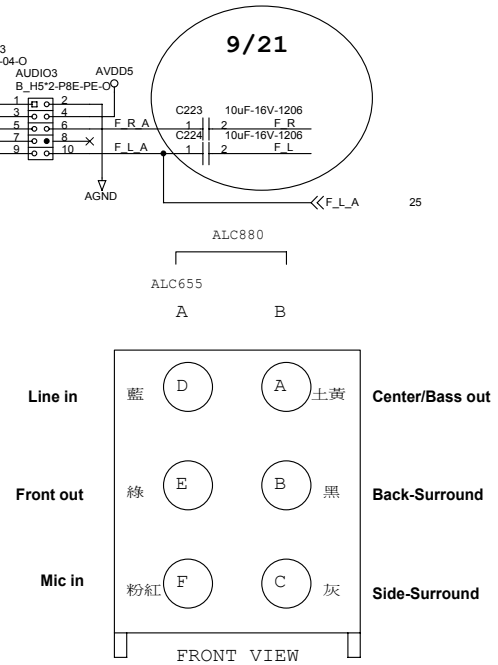
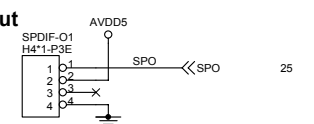


SPDIF I/O

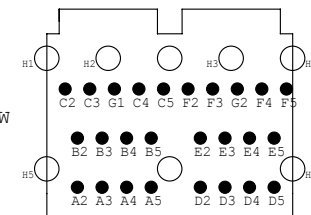
SPDIF In

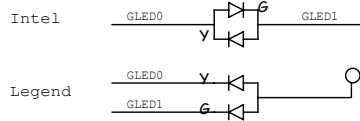
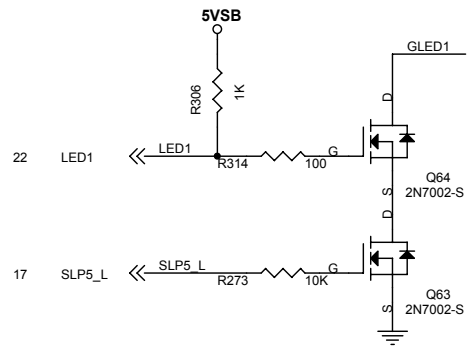
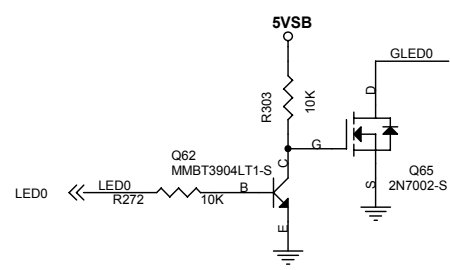
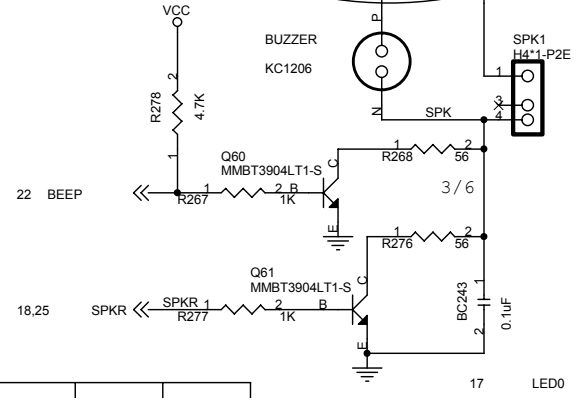
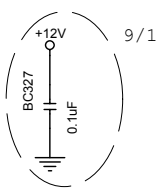
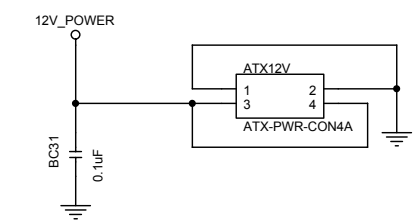
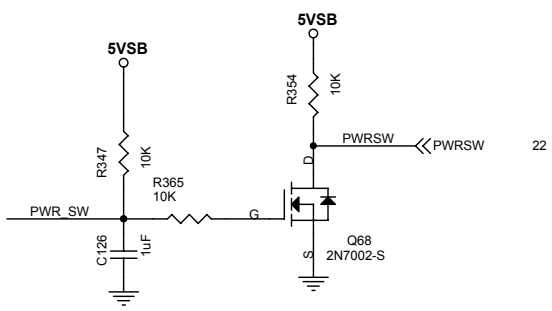
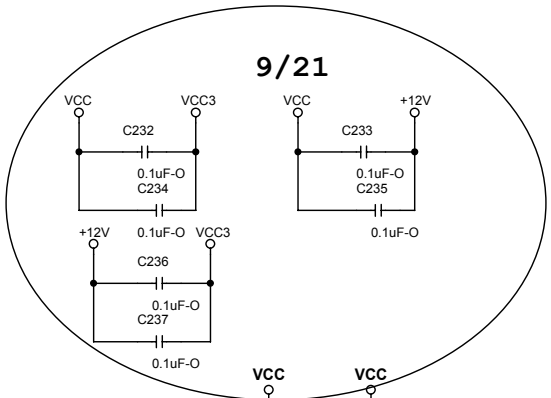
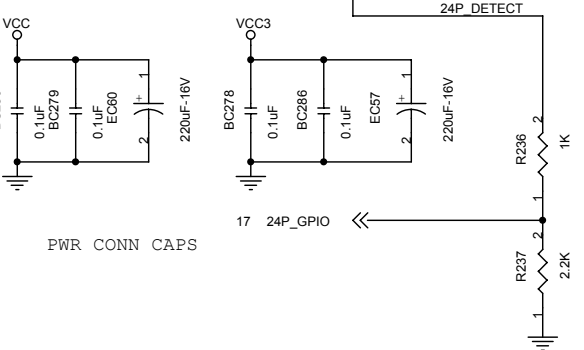
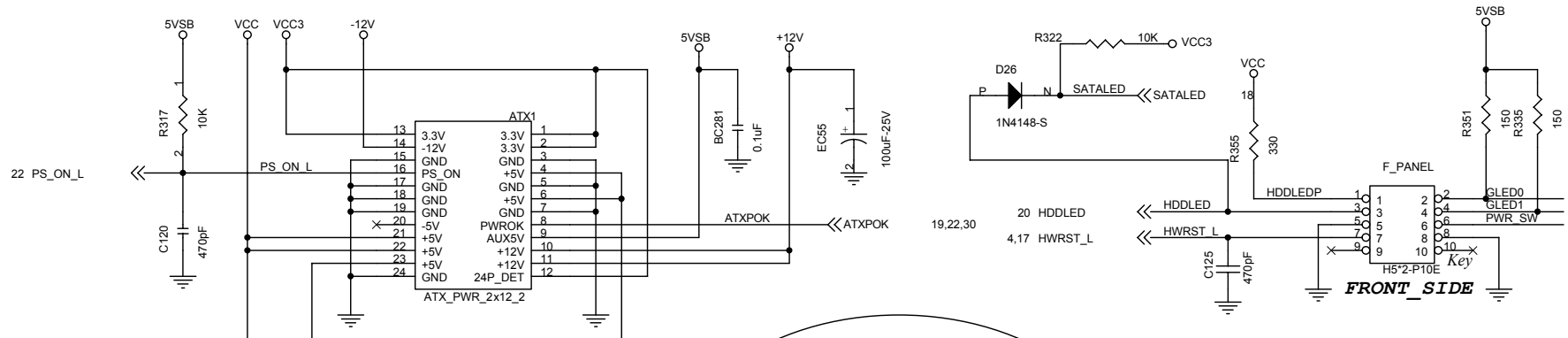


SPDIF Out

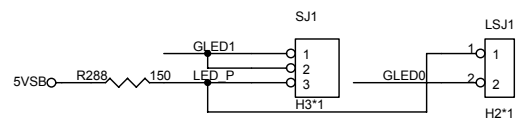


TOP VIEW





	S0	S1	S3	S4,S5
PANEL1 (4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1 (3,5,7)	Green	G-blinking	G-blinking	Dark
LSJ1 (1,2)	Dark	Dark	Light	Dark
SJ1 (1,3) (2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH

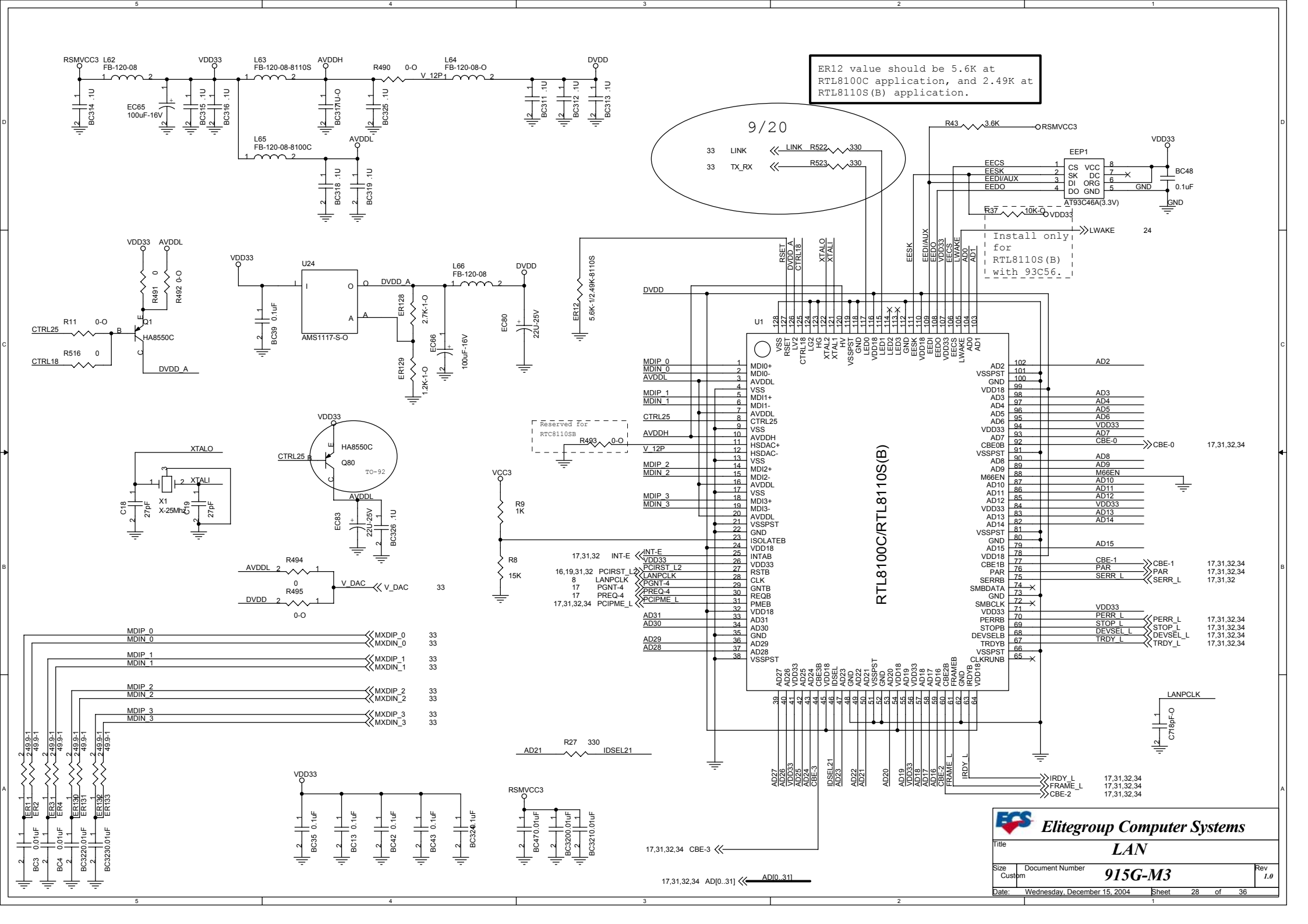


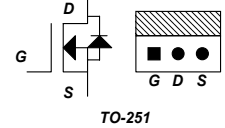
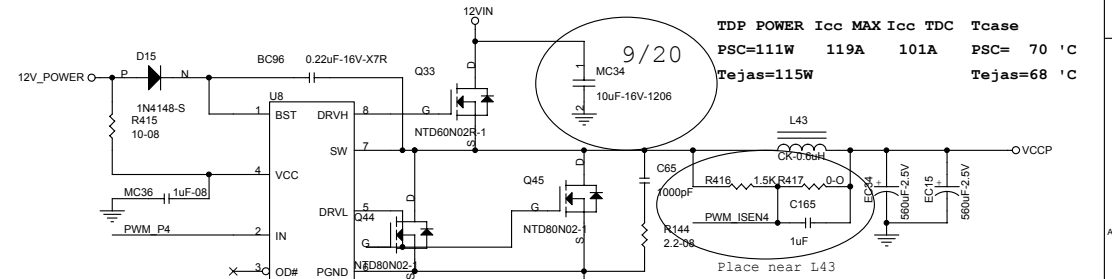
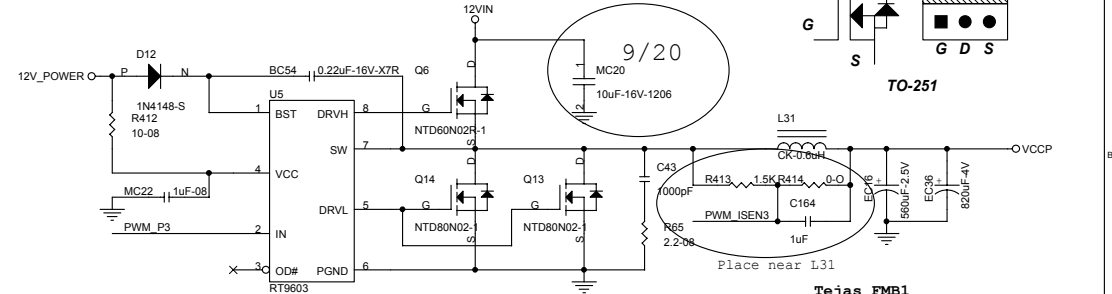
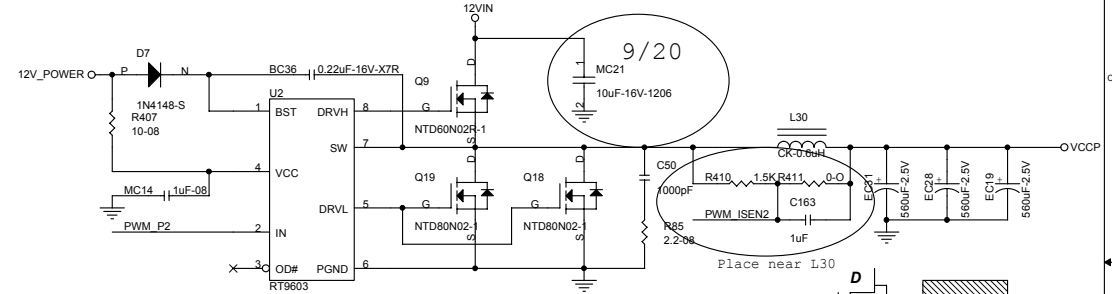
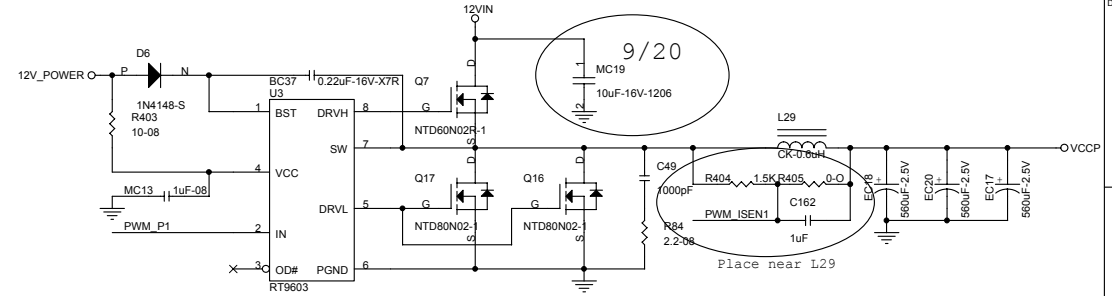
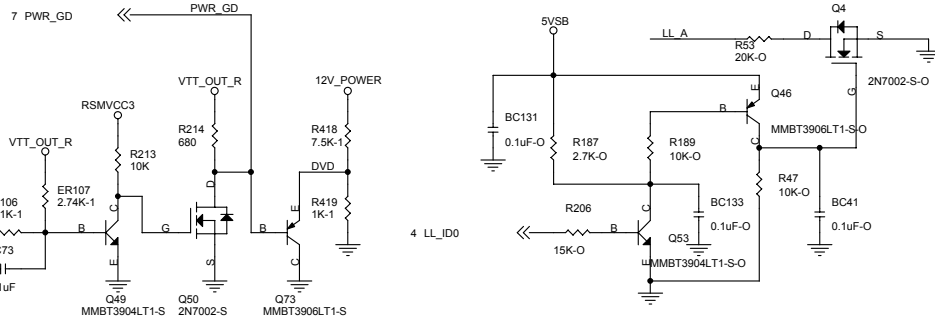
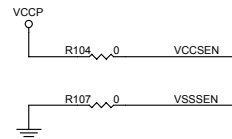
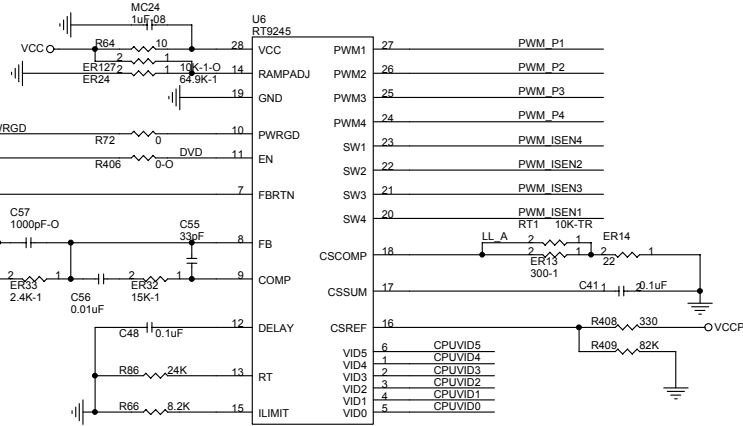
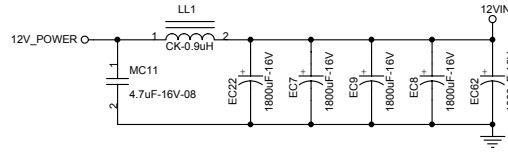
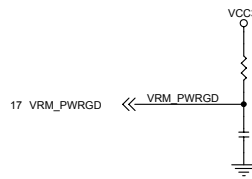
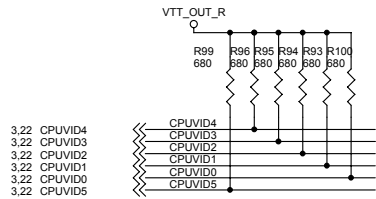
Elitegroup Computer Systems

ATX Power & Front Panel

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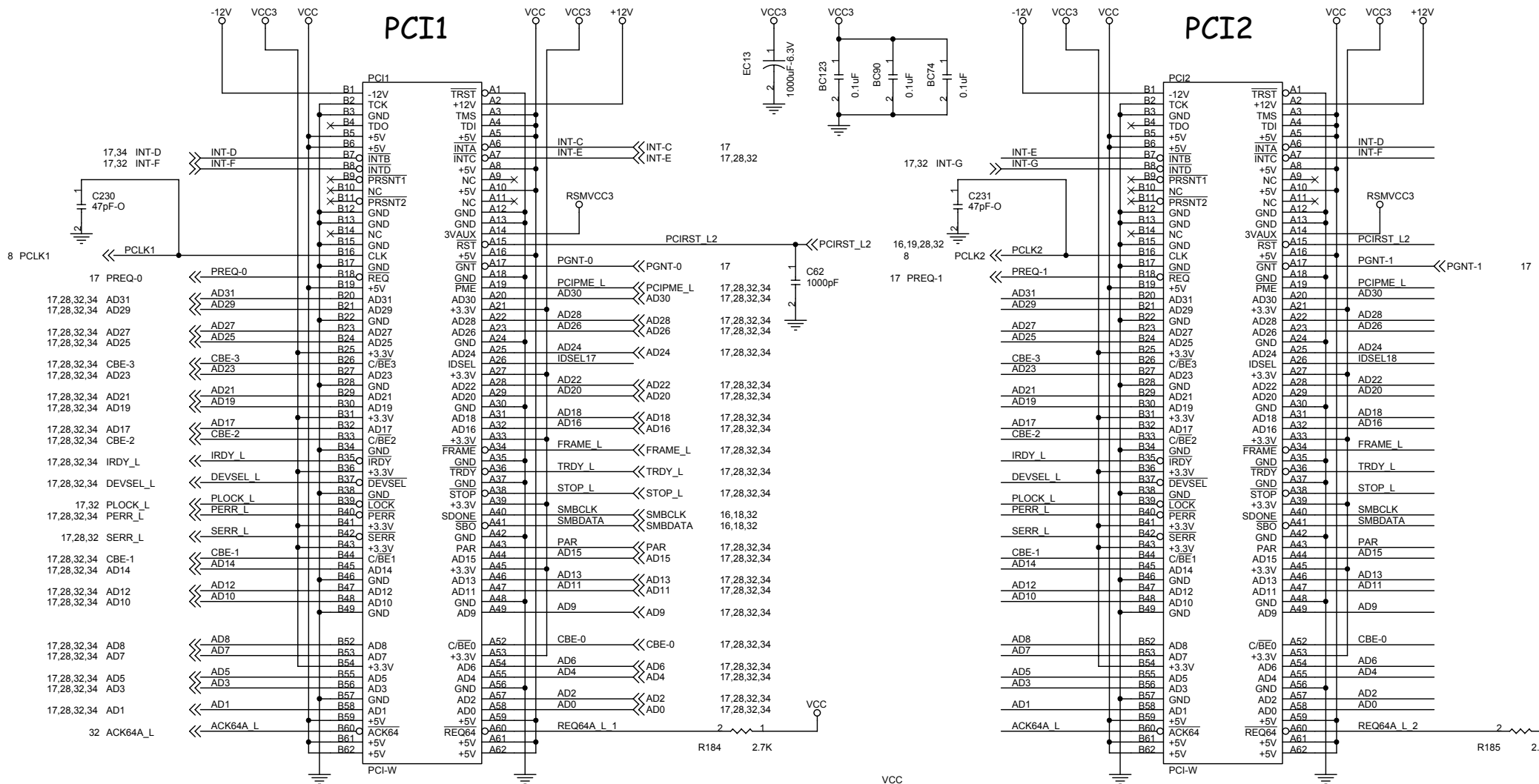


Tejas FMB1

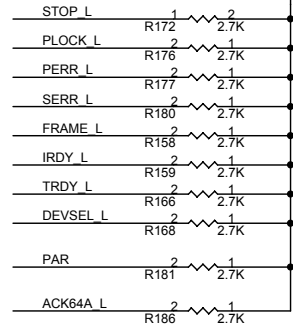
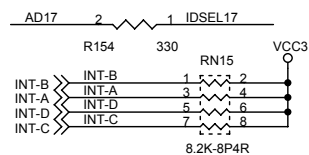
TDP POWER	Icc MAX	Icc TDC	Tc case
PSC=111W	119A	101A	PSC= 70 'C
Tejas=115W			Tejas=68 'C

PCI1

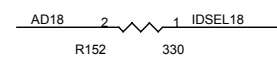
PCI2



PCI1-INT: IDSEL=AD17
 INTA:INTC REQ=PREQ0#
 INTB:INTD GNT=PGNT0#
 INTC:INTE
 INTD:INTF

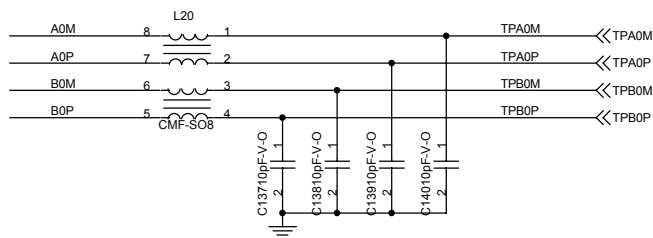


PCI2-INT: IDSEL=AD18
 INTA:INTD REQ=PREQ1#
 INTB:INTE GNT=PGNT1#
 INTC:INTF
 INTD:INTG

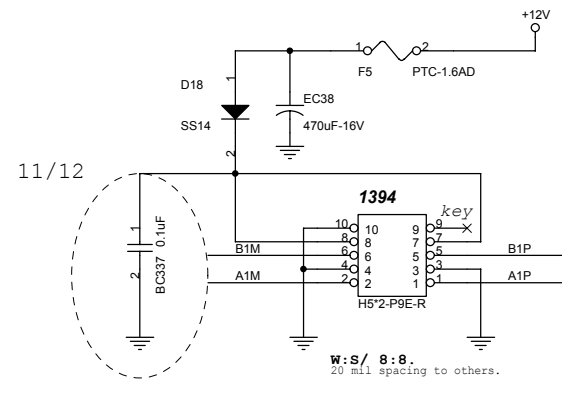
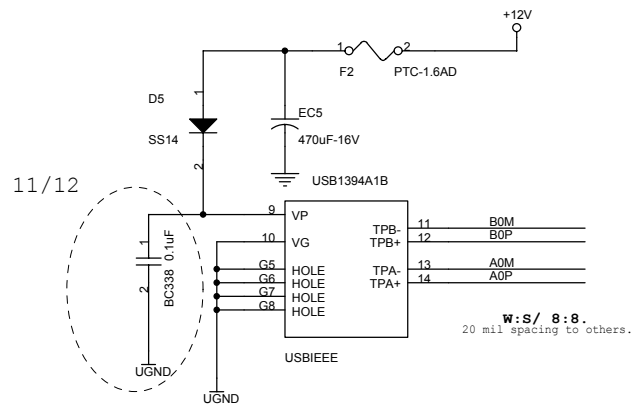
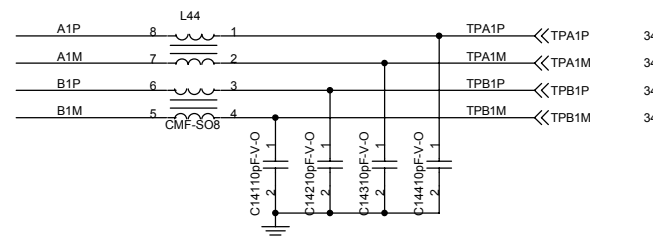


Title PCI Slot 1&2	
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B0P	R370	0-O	TPB0P
B0M	R372	0-O	TPB0M
A0P	R374	0-O	TPA0P
A0M	R376	0-O	TPA0M



B1M	R371	0-O	TPB1M
B1P	R373	0-O	TPB1P
A1M	R375	0-O	TPA1M
A1P	R377	0-O	TPA1P



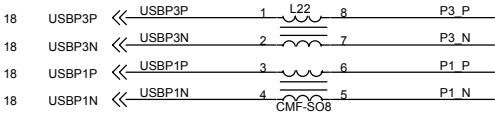
REAR_SIDE

USBP0N	R378	0-O	P0_N
USBP0P	R380	0-O	P0_P
USBP2N	R382	0-O	P2_N
USBP2P	R384	0-O	P2_P

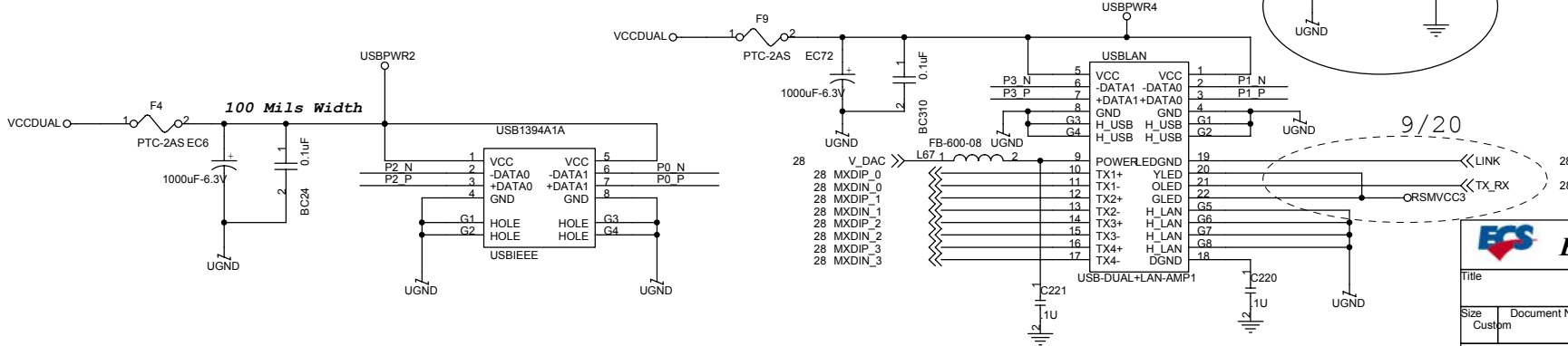
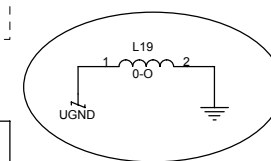


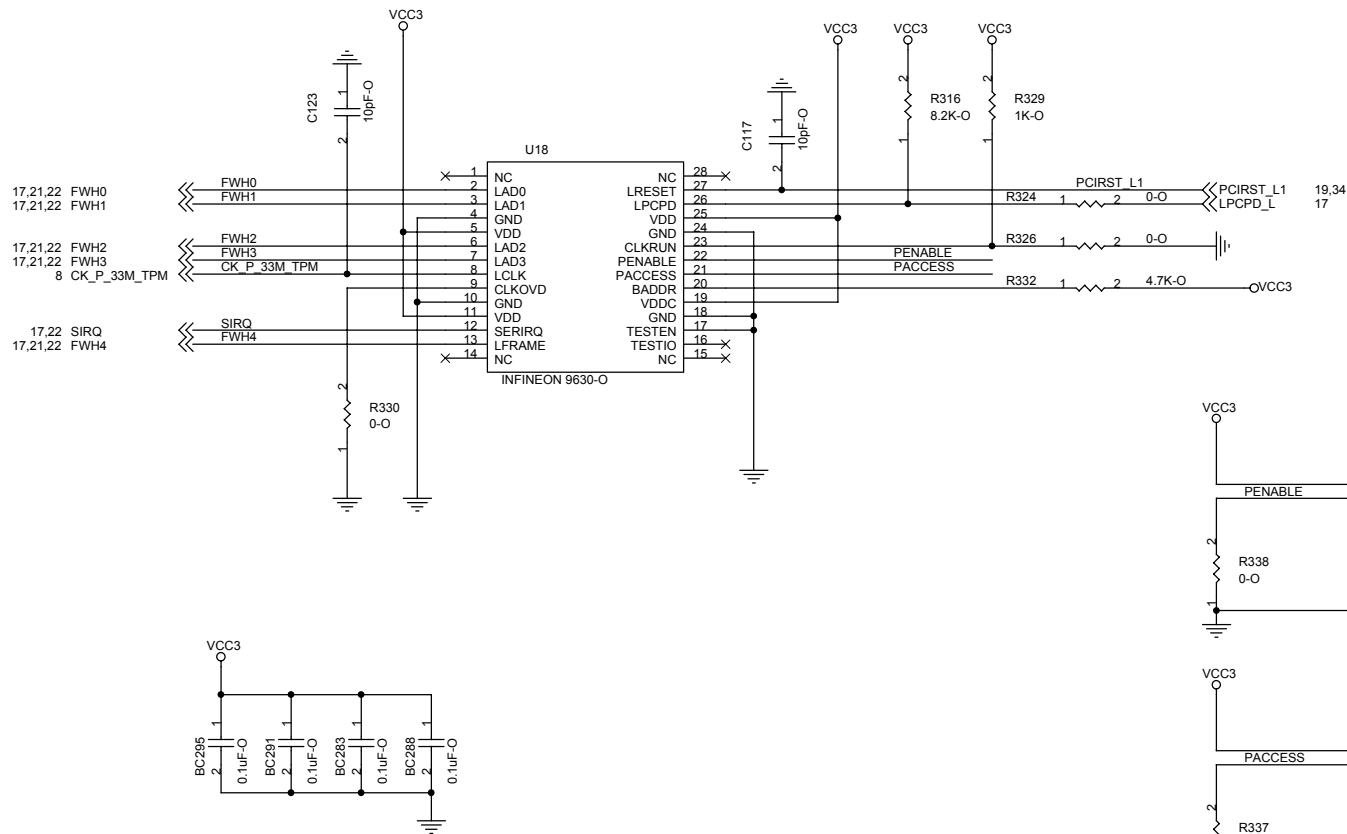
REAR_SIDE

USBP1N	R379	0-O	P1_N
USBP1P	R381	0-O	P1_P
USBP3N	R383	0-O	P3_N
USBP3P	R385	0-O	P3_P




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1	2	3	4	5	6	7	8
A							A
B							B
C							C
D							D

 Elitegroup Computer Systems		
Title		
Schematic Change History		
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